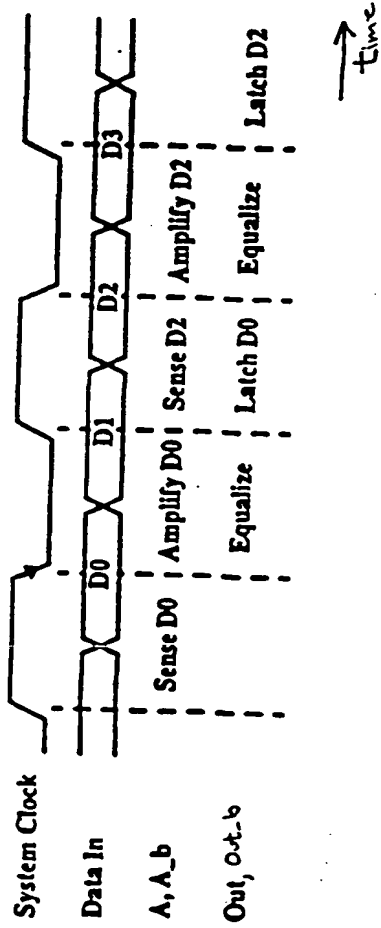


Prior Art

FIG 1



Pror Art

FIG. 2

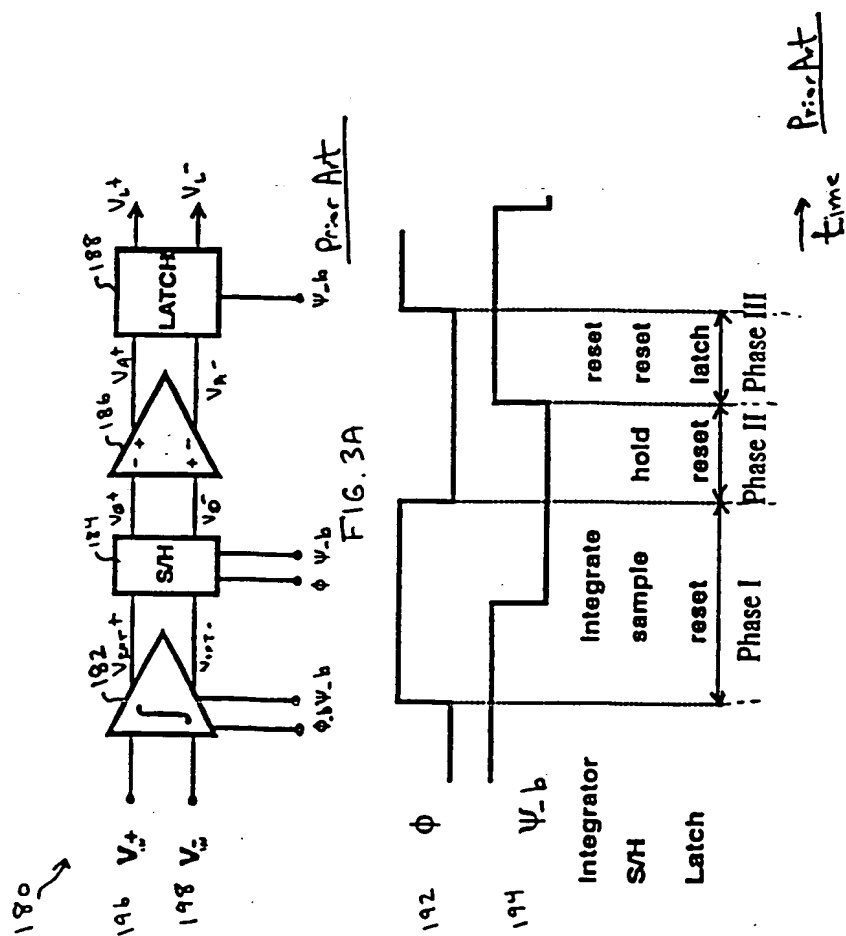


FIG. 4

Prior Art

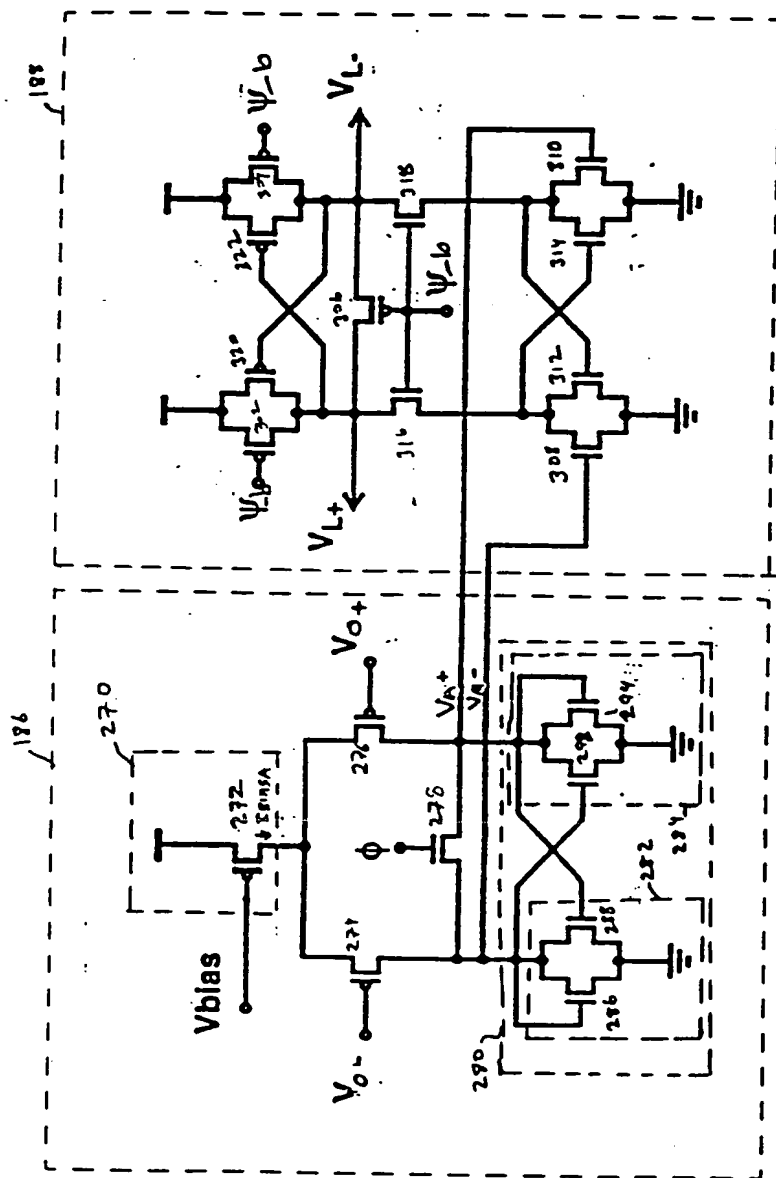


FIG. 5

Proc. ASCE

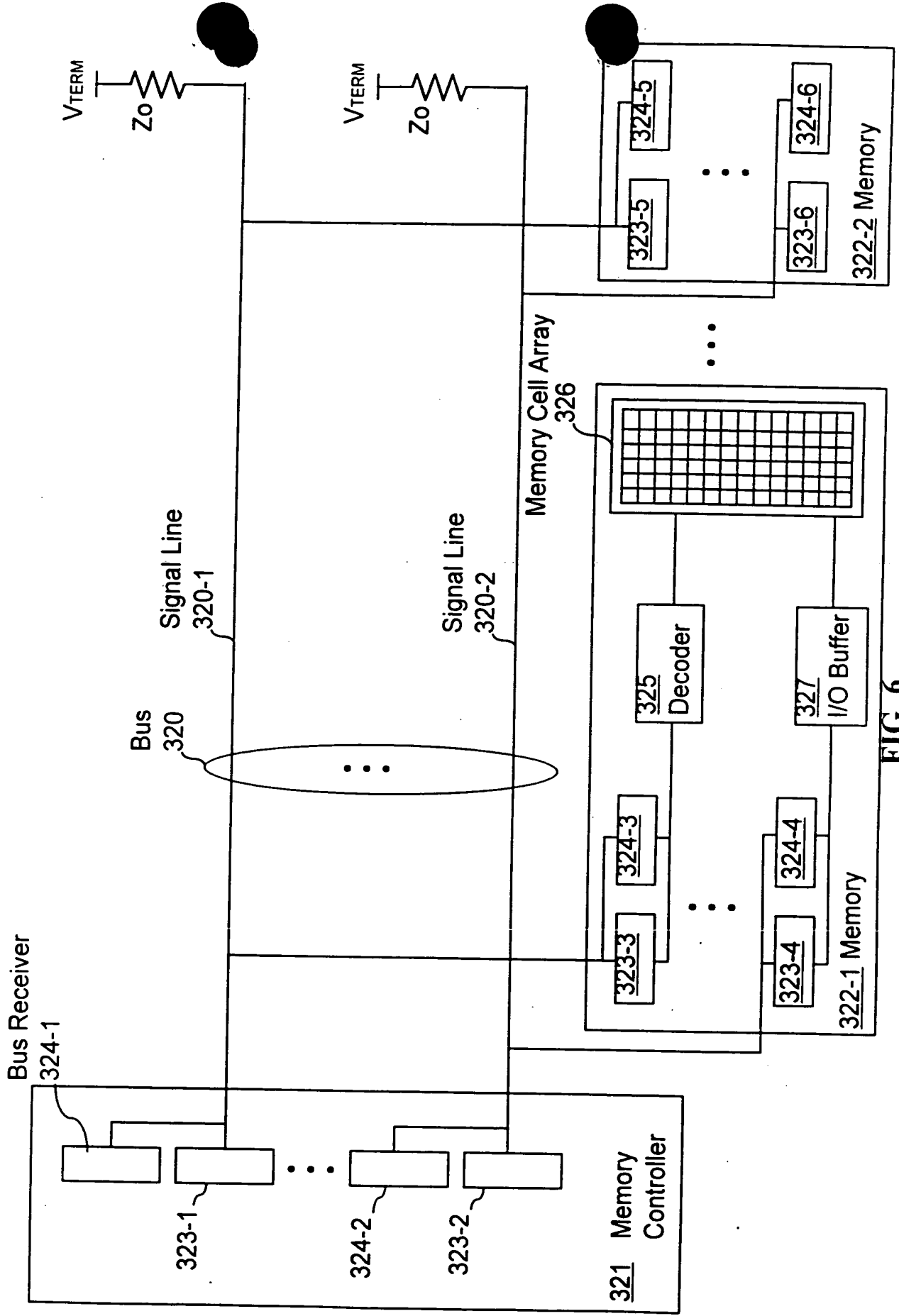


FIG. 6

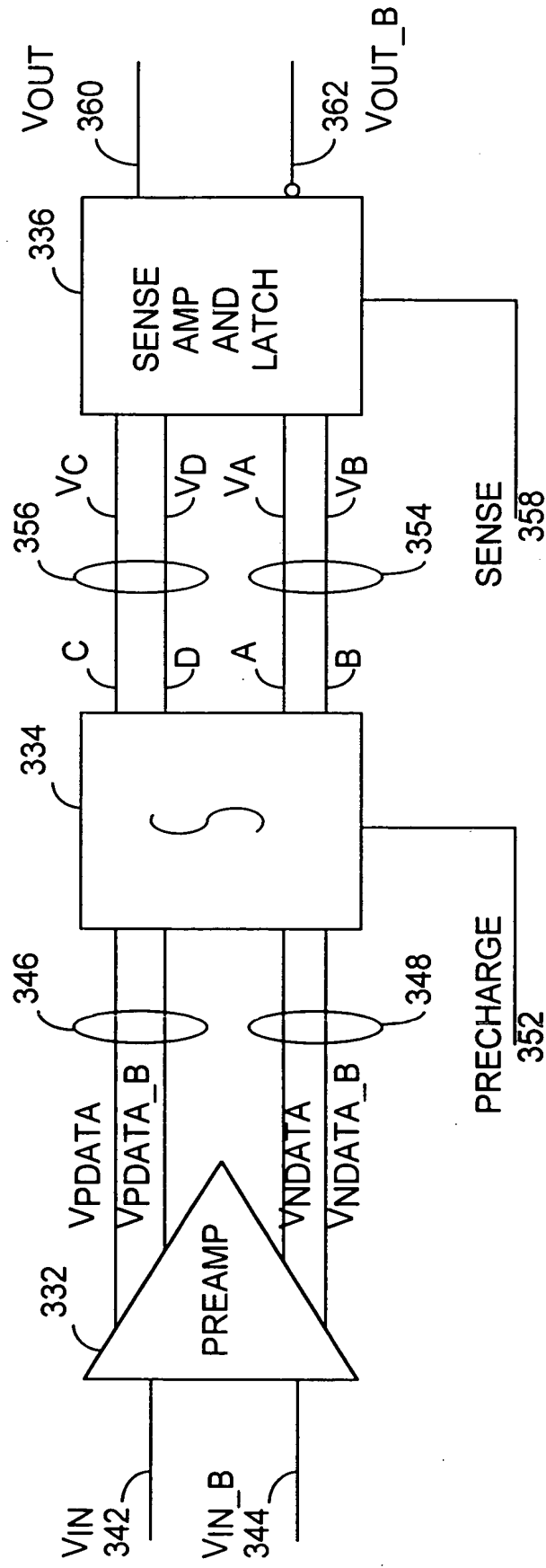


FIG. 7A

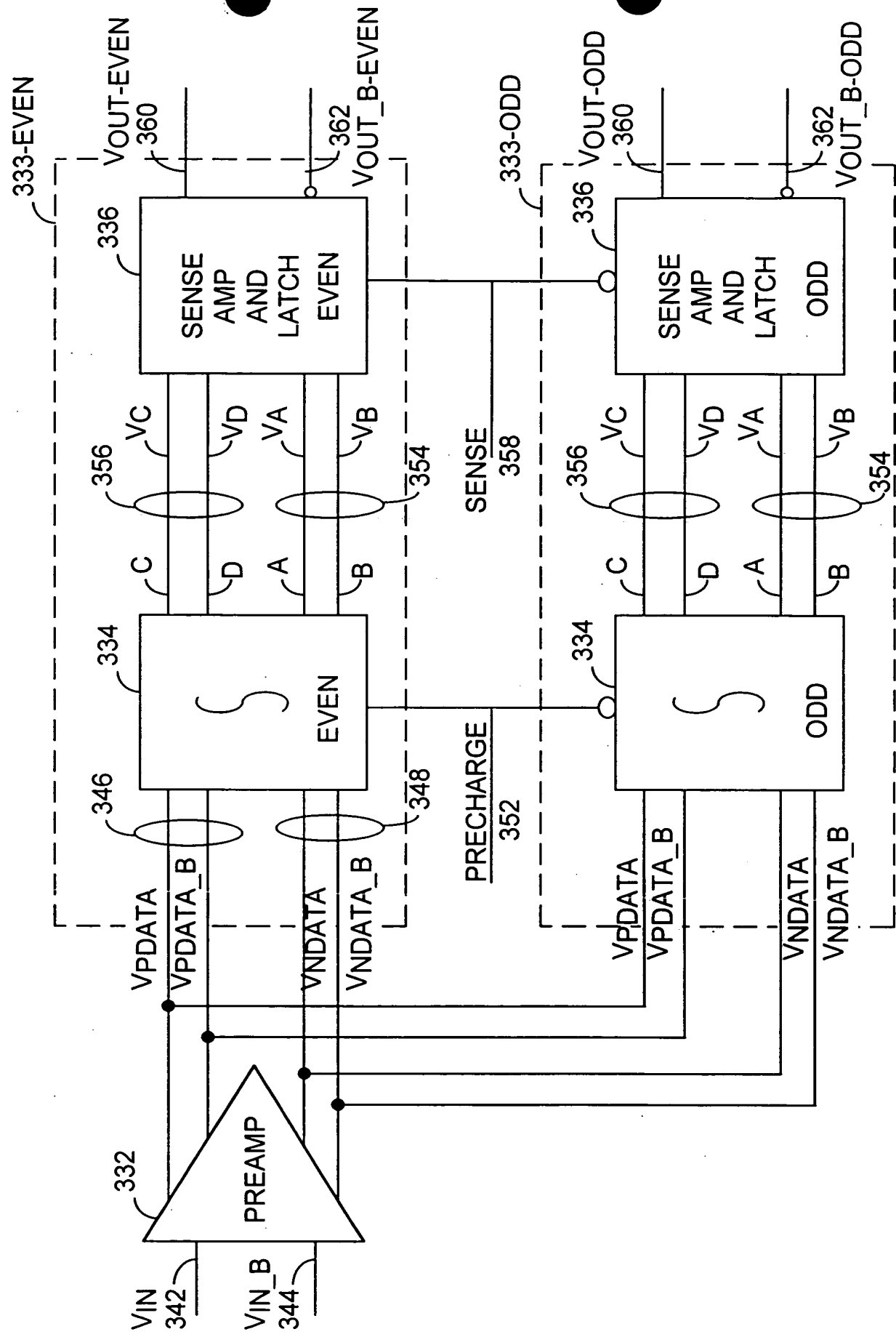


FIG. 7B

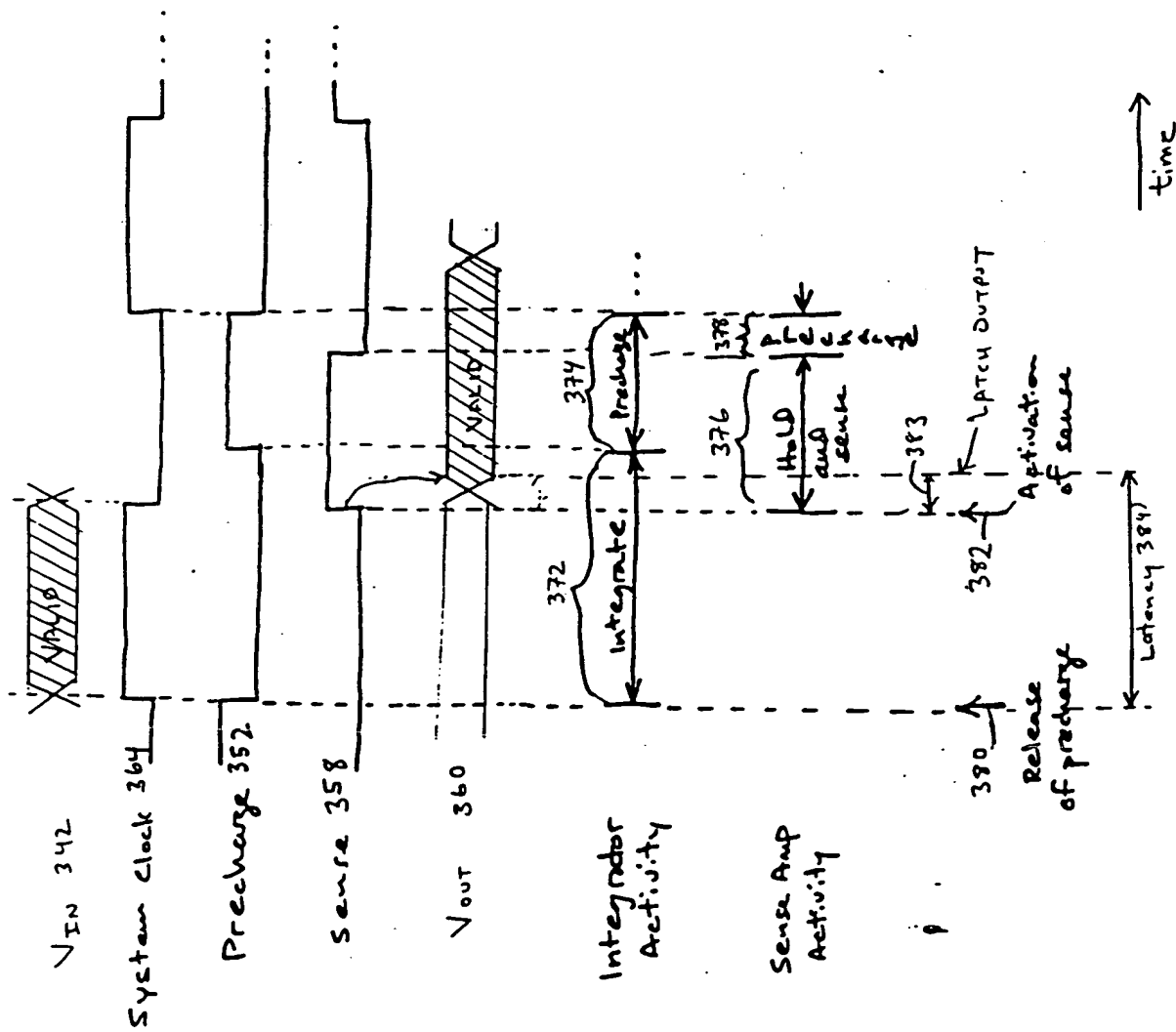


FIG. 8

390

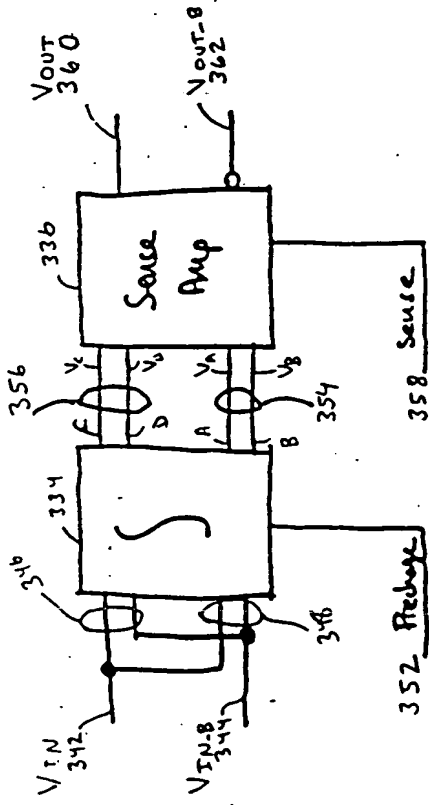


FIG. 9

334A

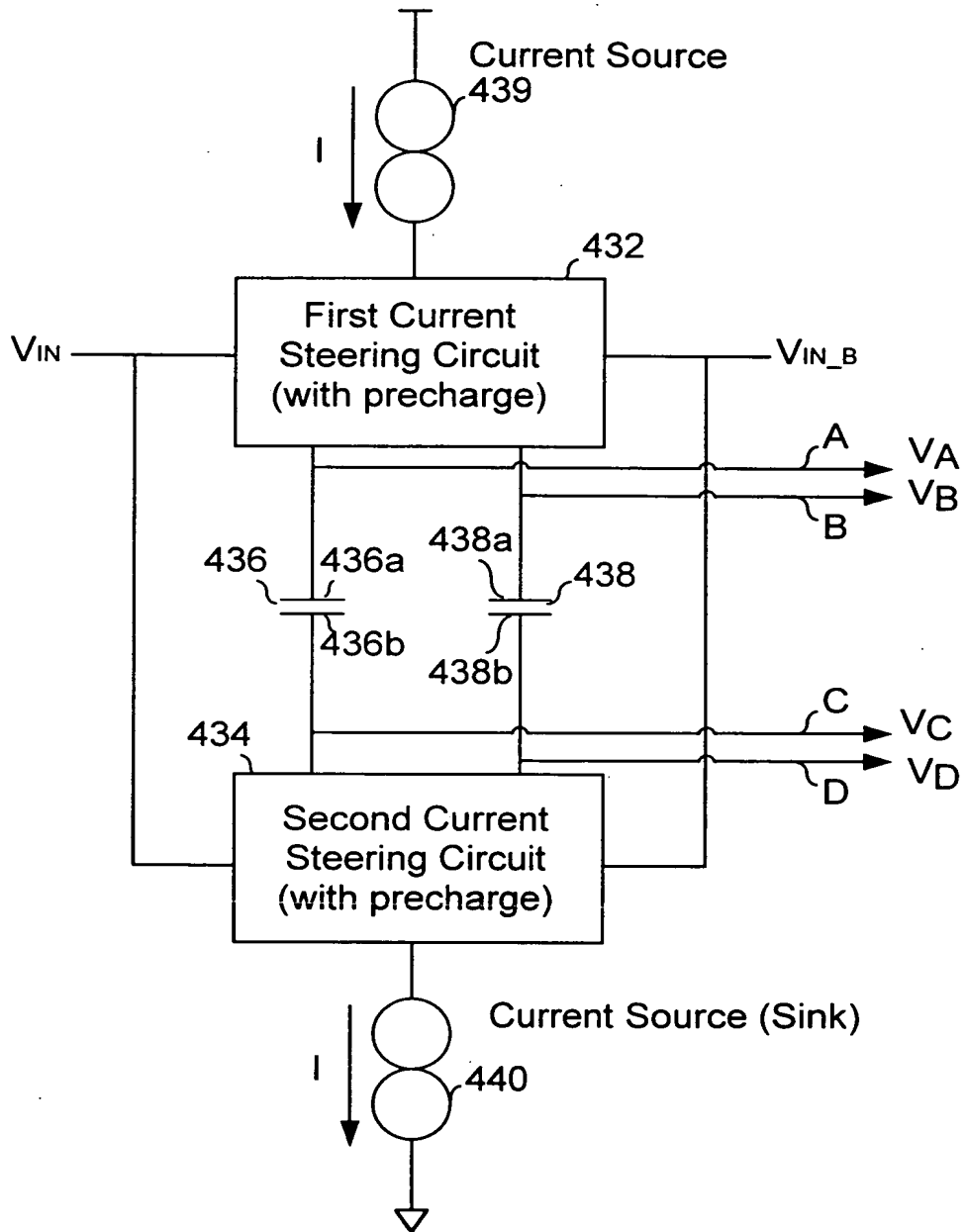


FIG. 11A

Integrator
334B

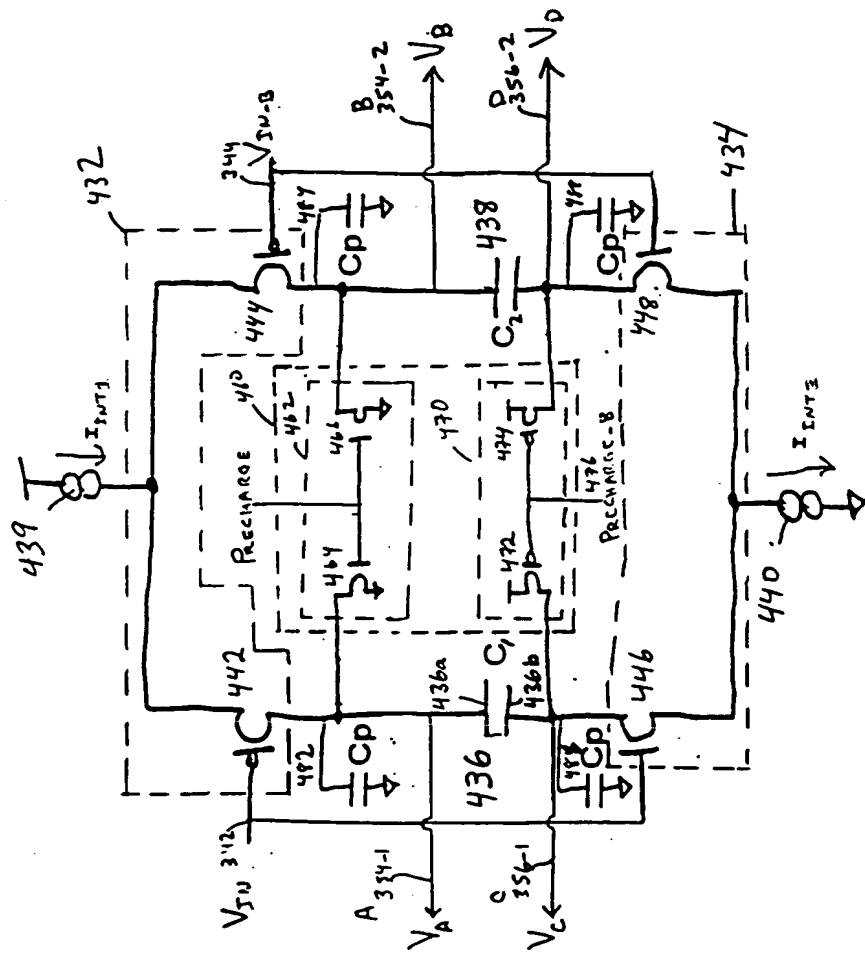


FIG. 11B

005070-97662160

Integrator
334C

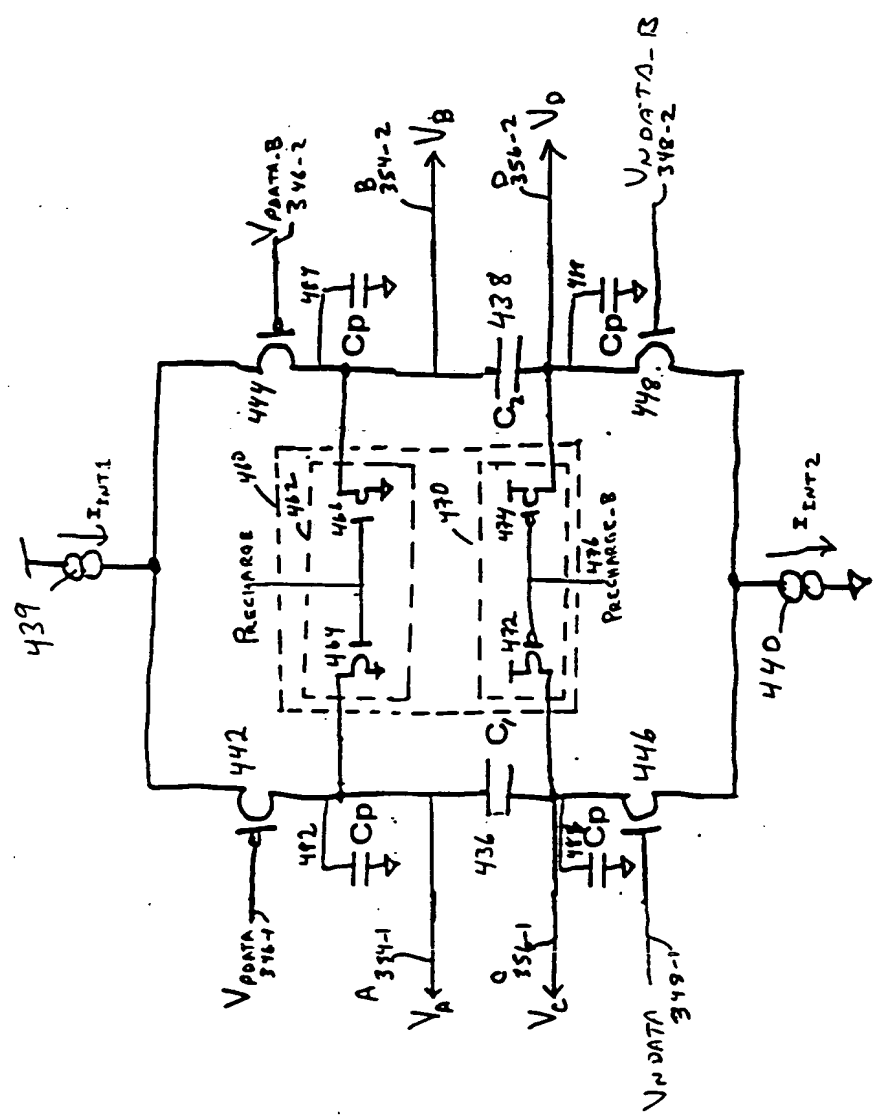


FIG. 11c

INTEGRATOR
334D

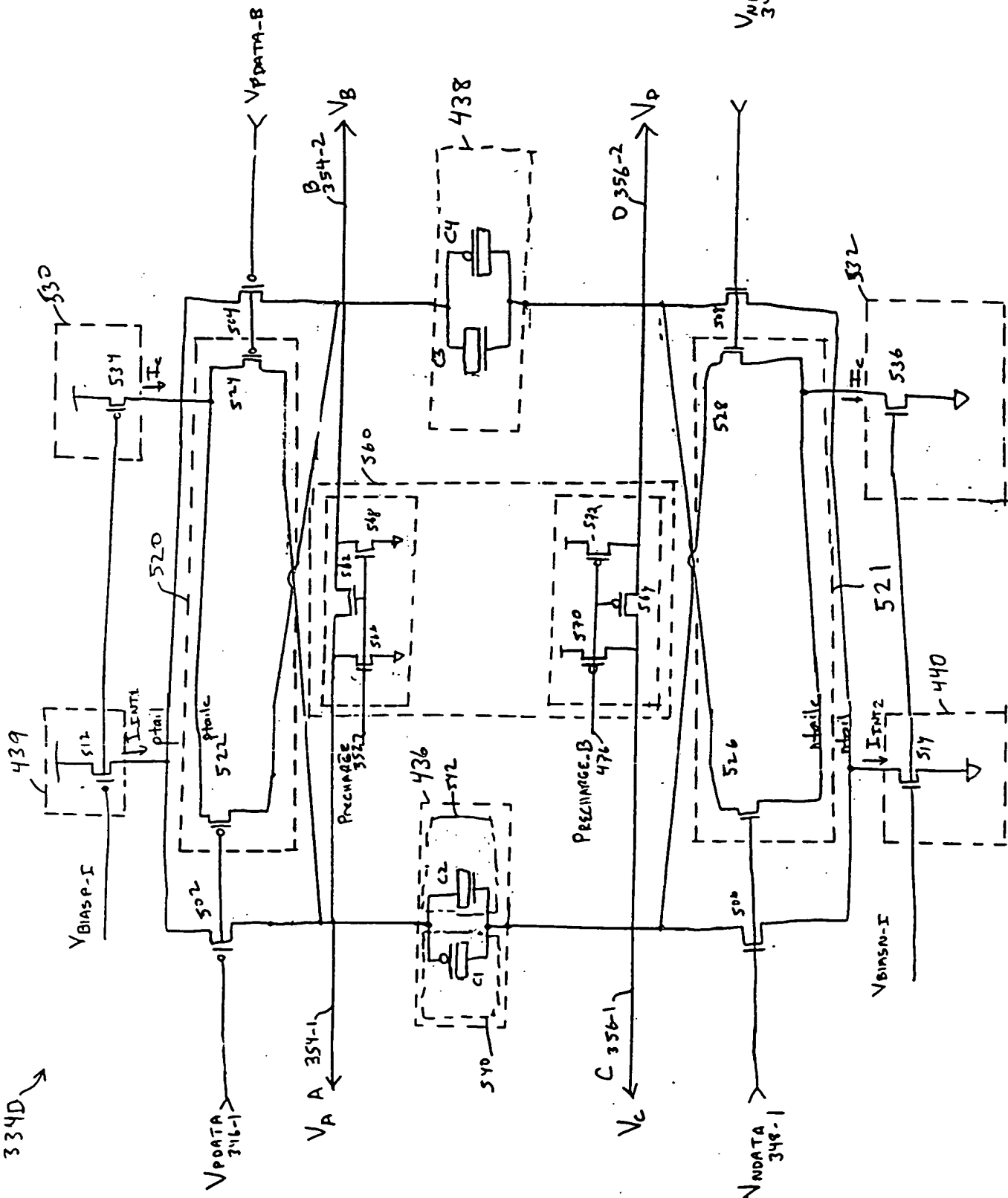


FIG. 12

Sense Amp Driver and Latch
336A

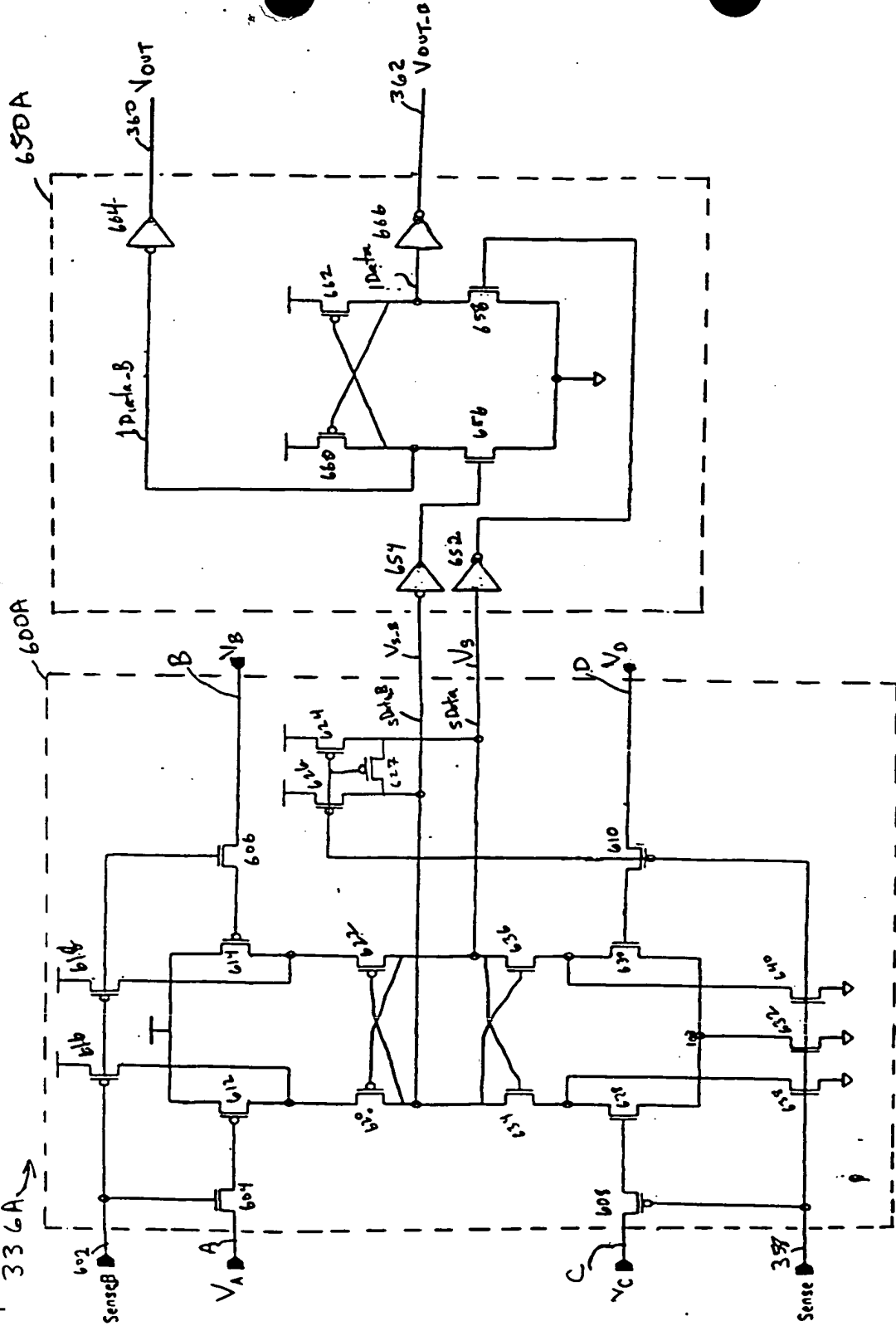


FIG. 14A

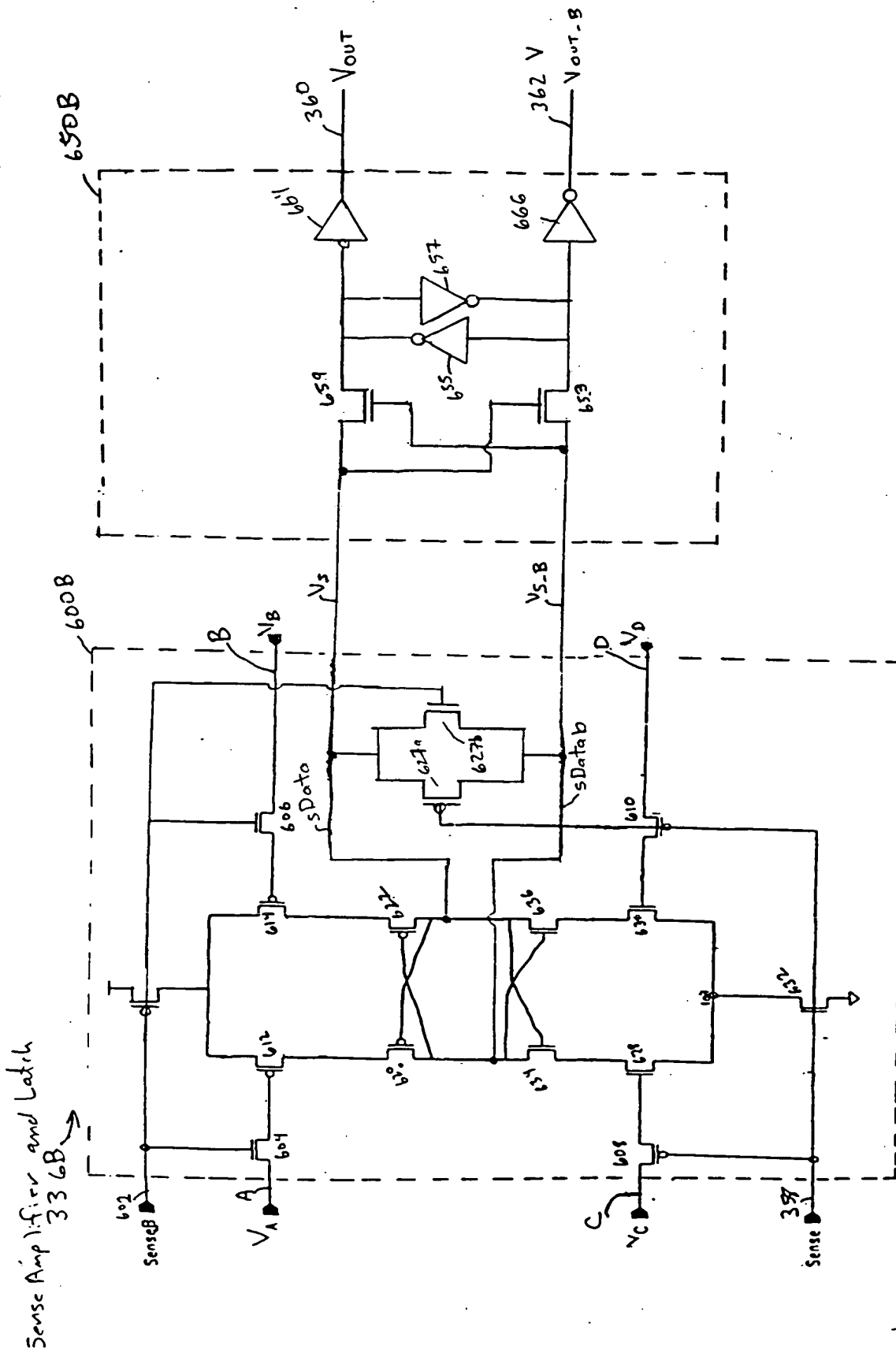


FIG. 14B

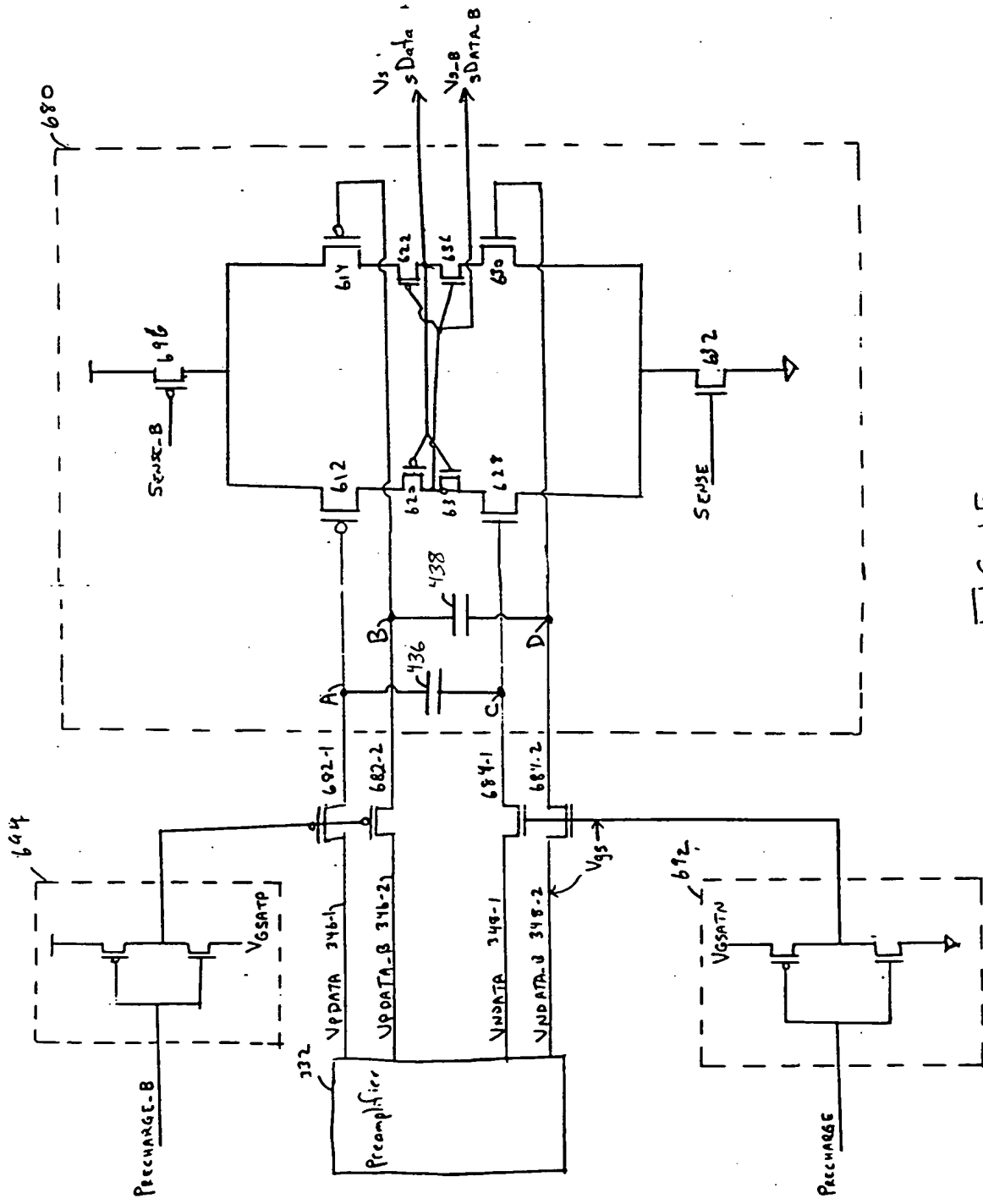


FIG. 15

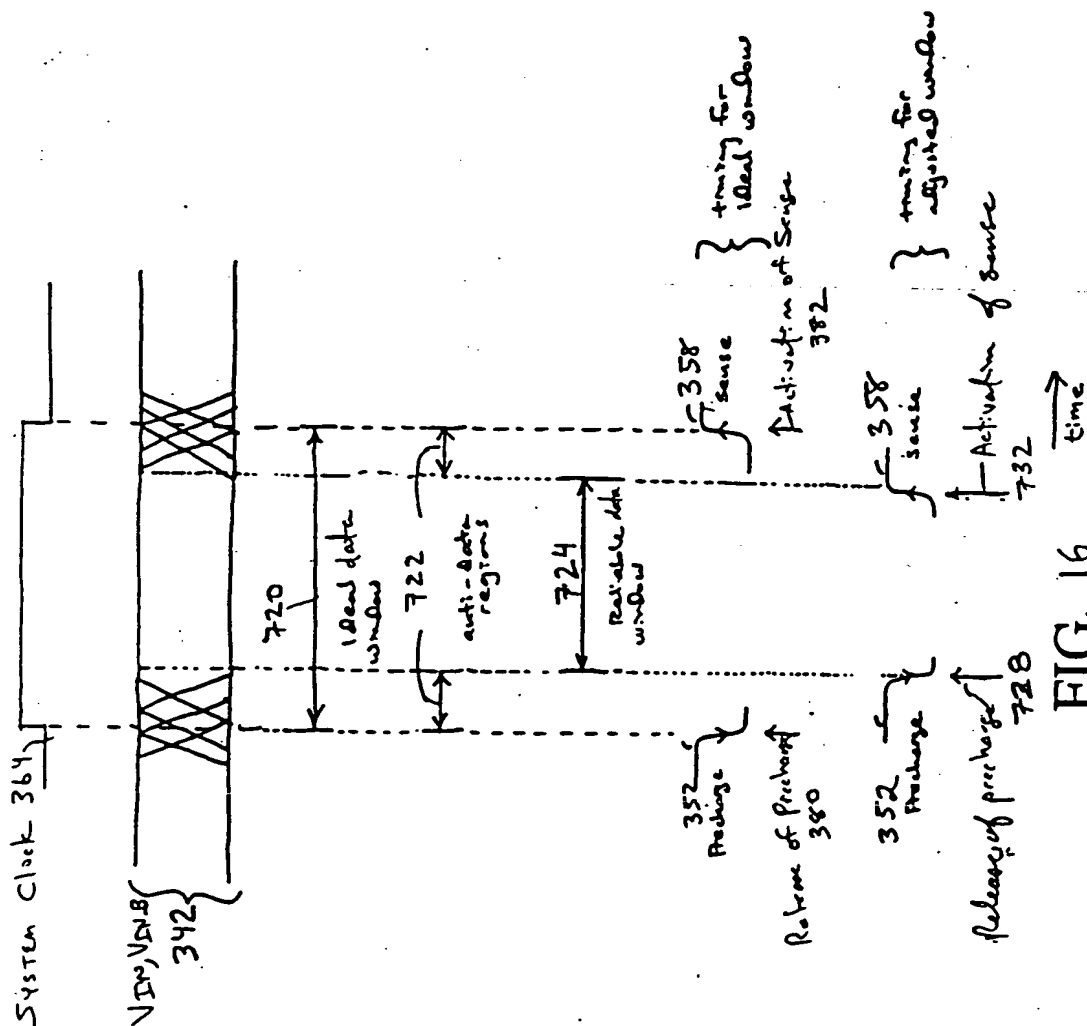


FIG. 16

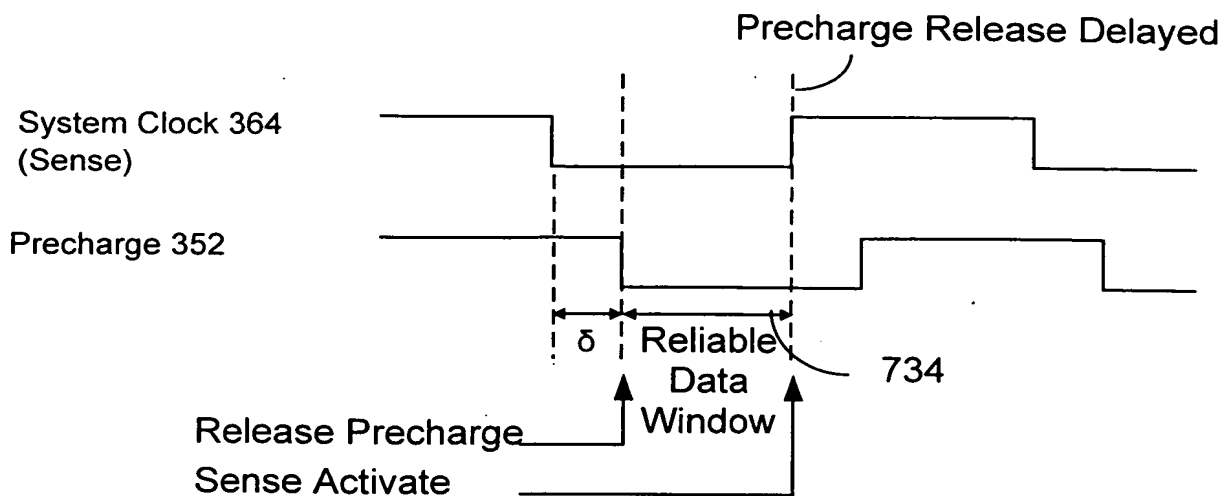


FIG. 17A

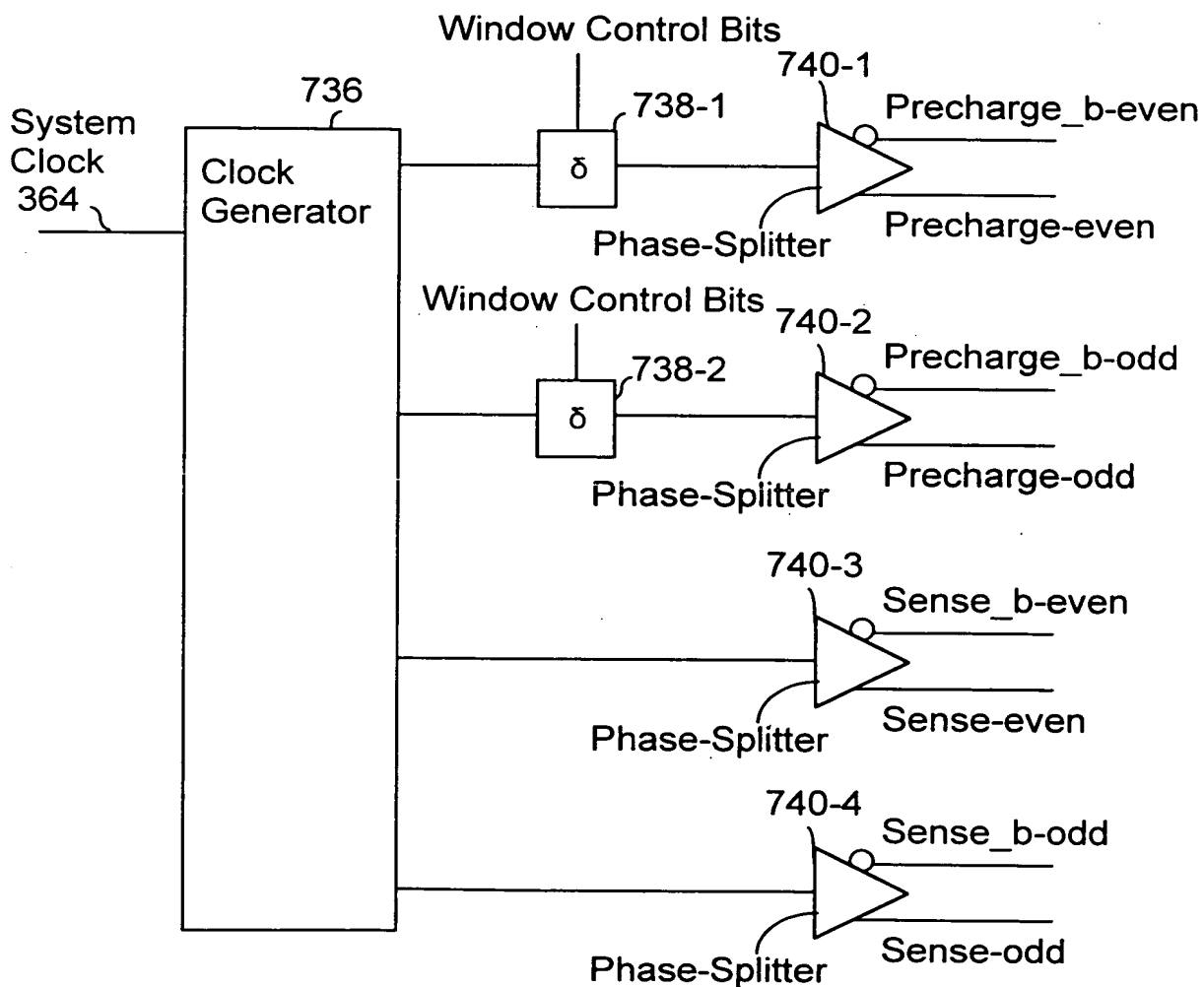
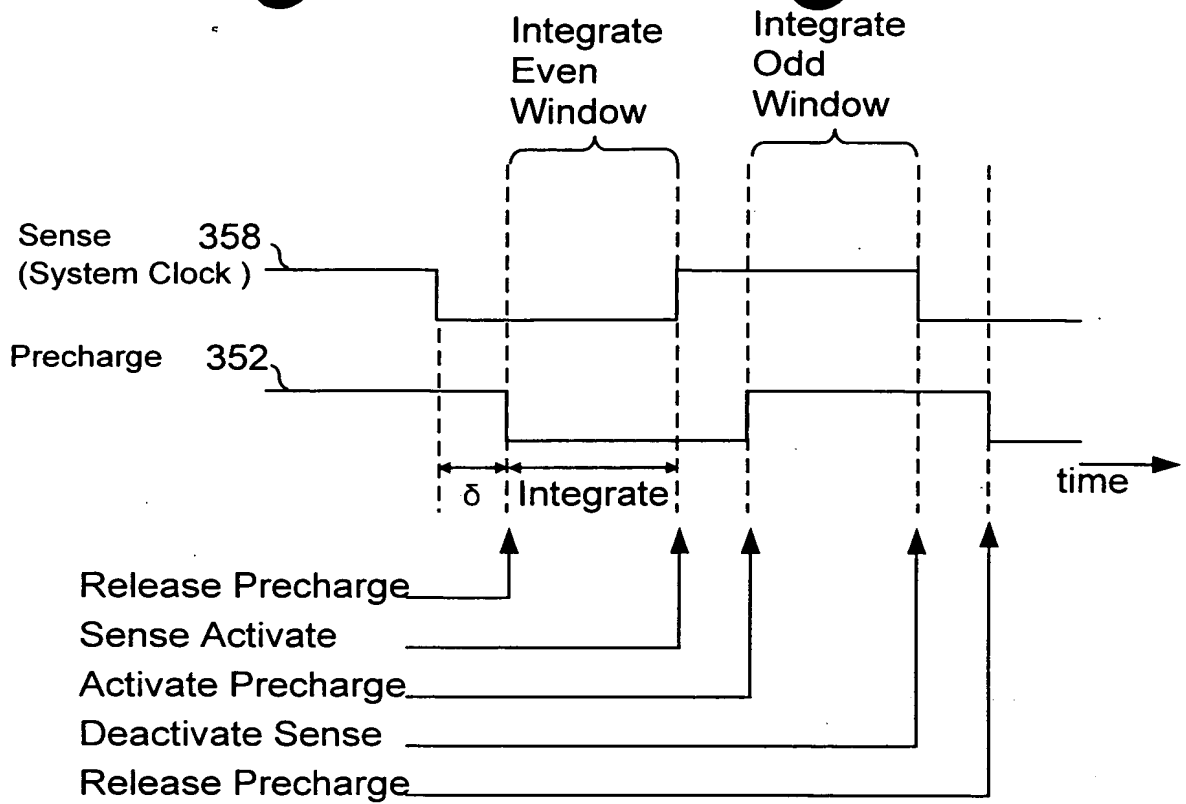
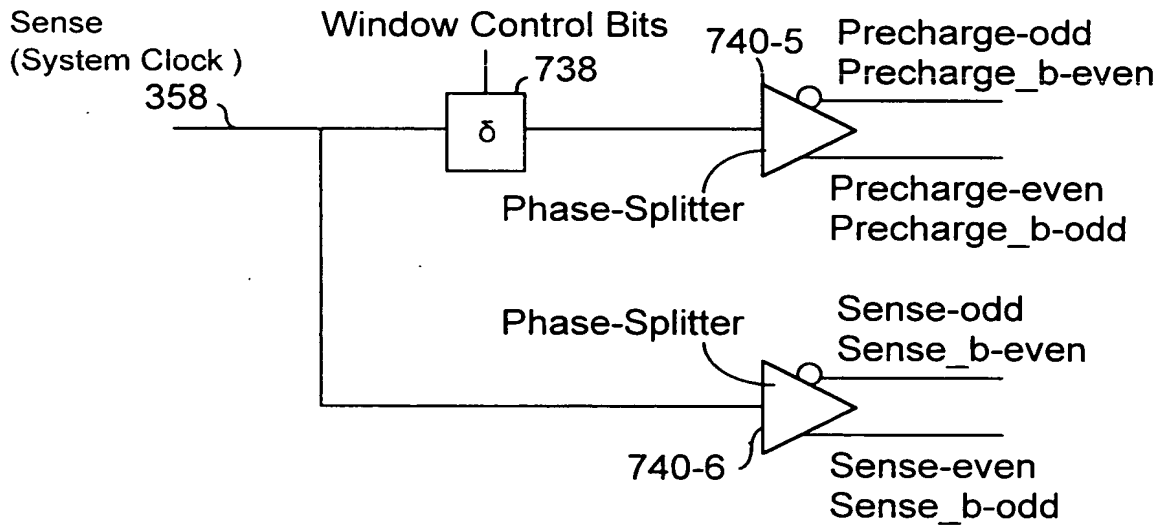


FIG. 17B

003070-9765460



Timing Diagram of Precharge and Sense Signals
FIG. 17C



Circuit for Timing Diagram of Fig. 17C
FIG. 17D

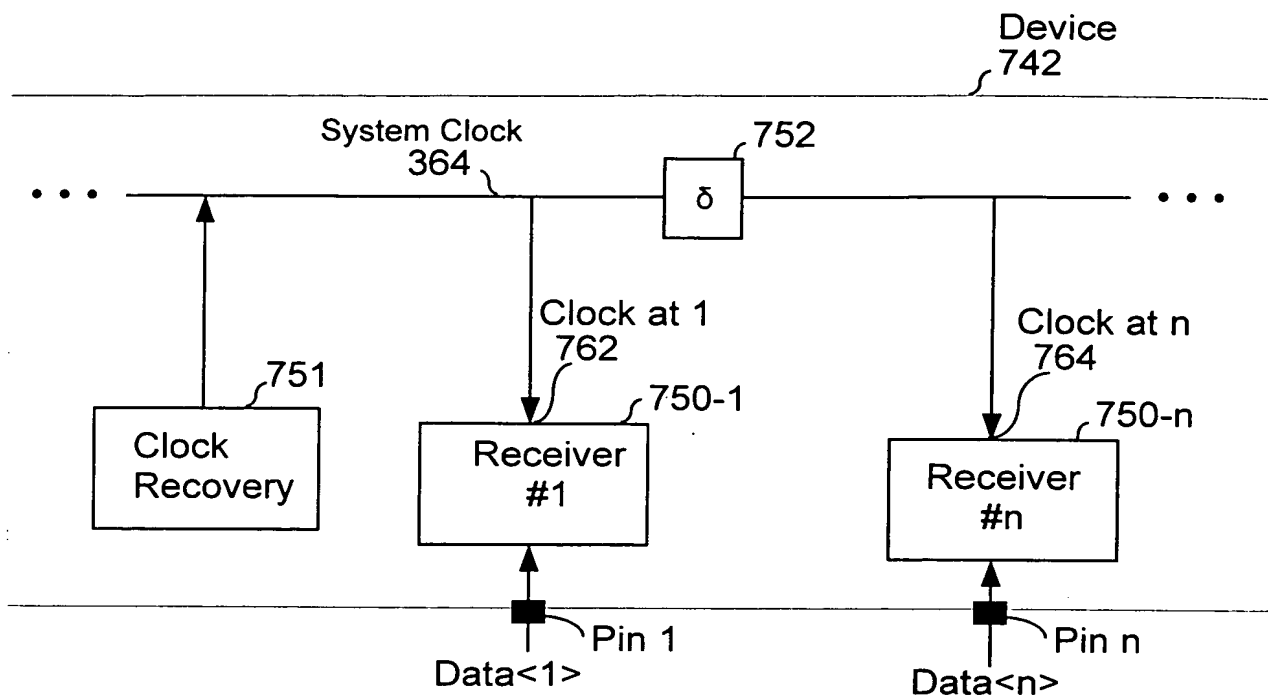


FIG. 18

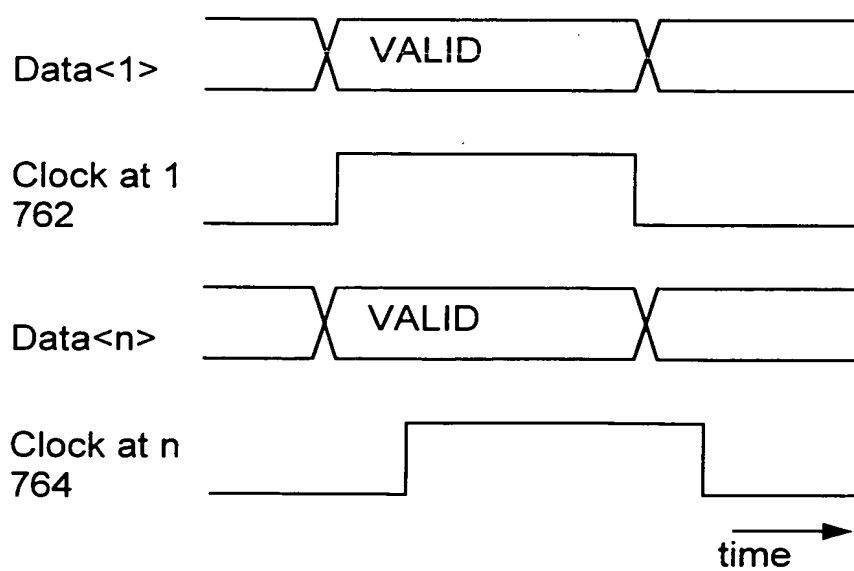


FIG. 19

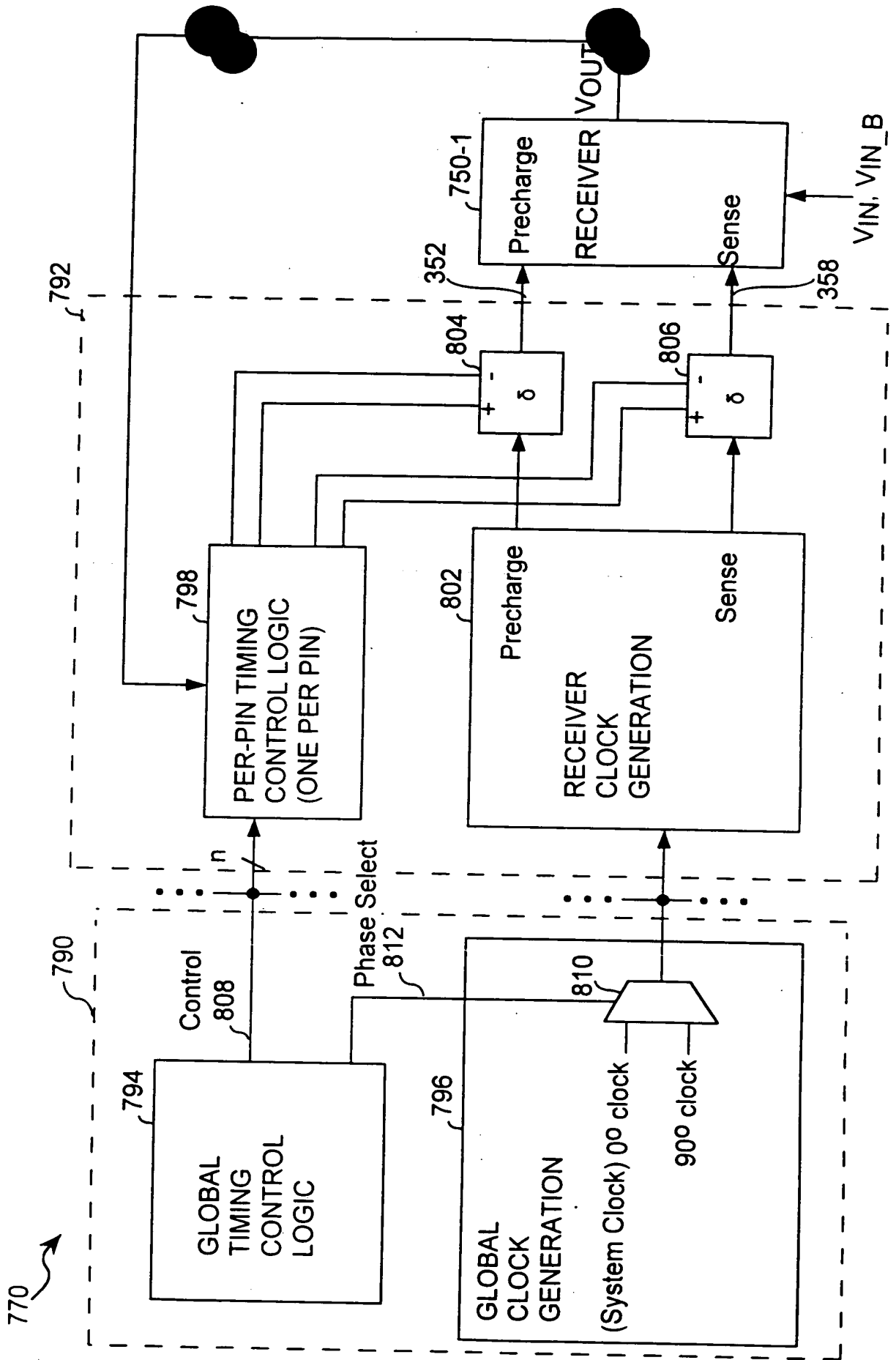


FIG. 20

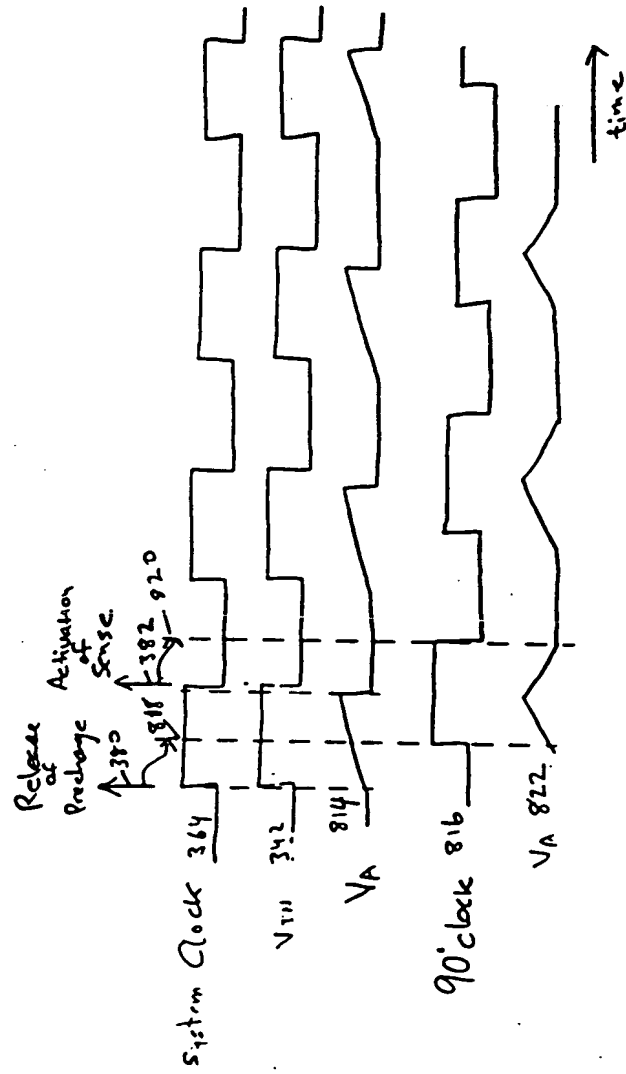
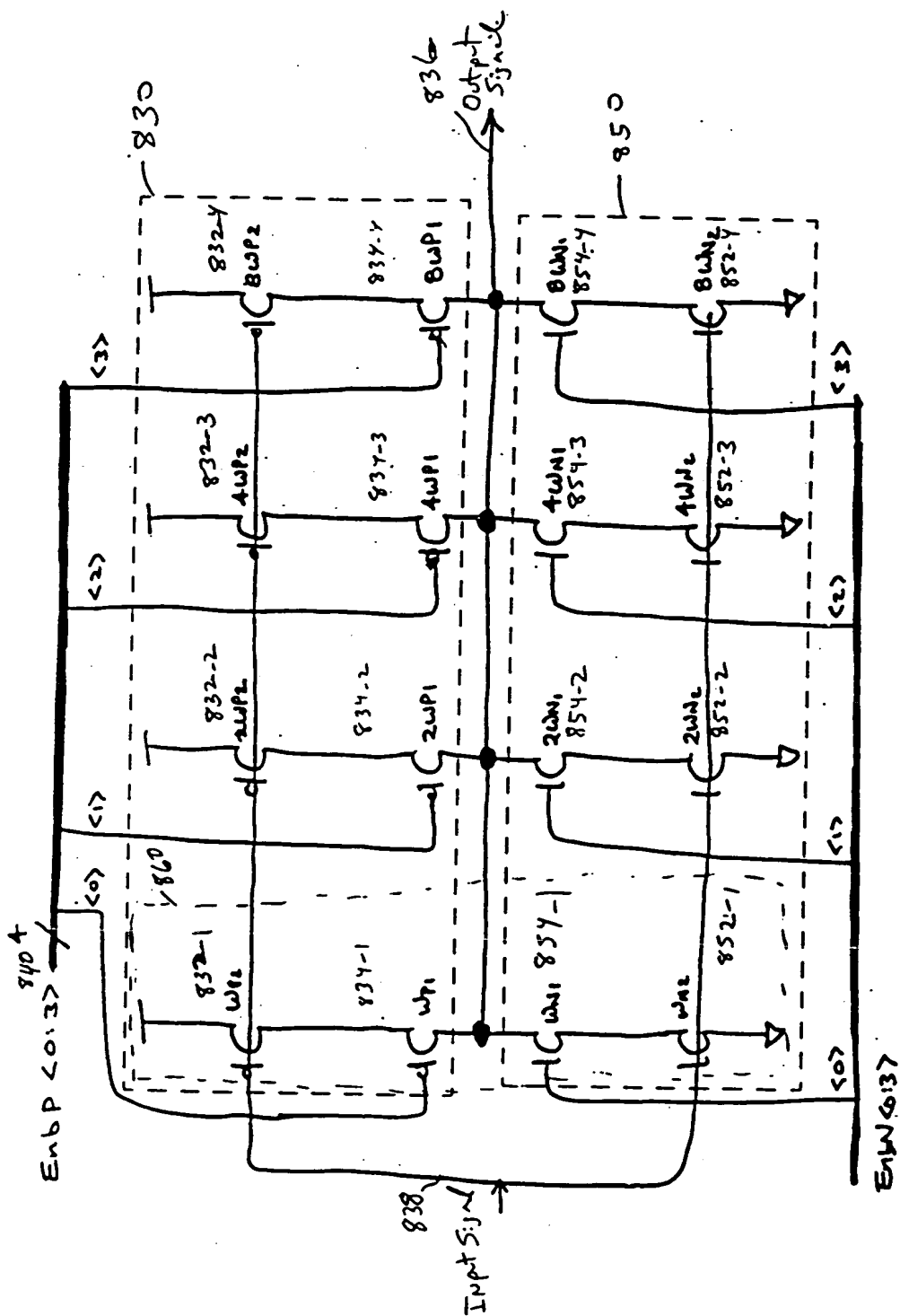


FIG. 21

804 ↗



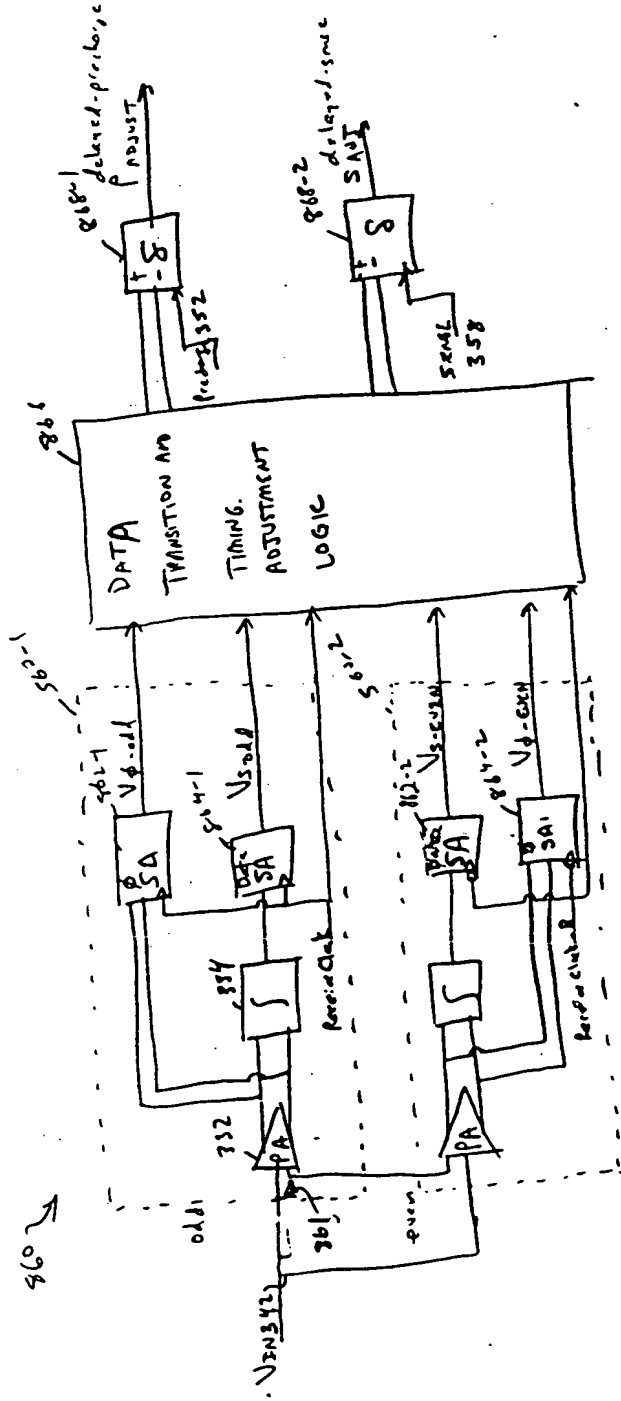


FIG. 23 A

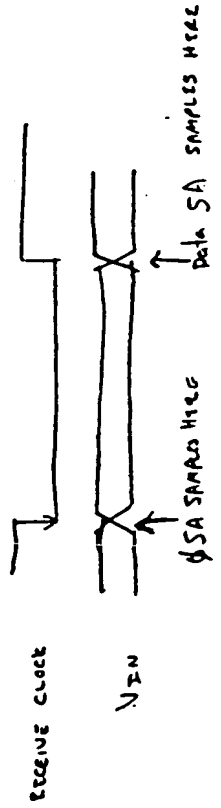


FIG. 23 B

870 →

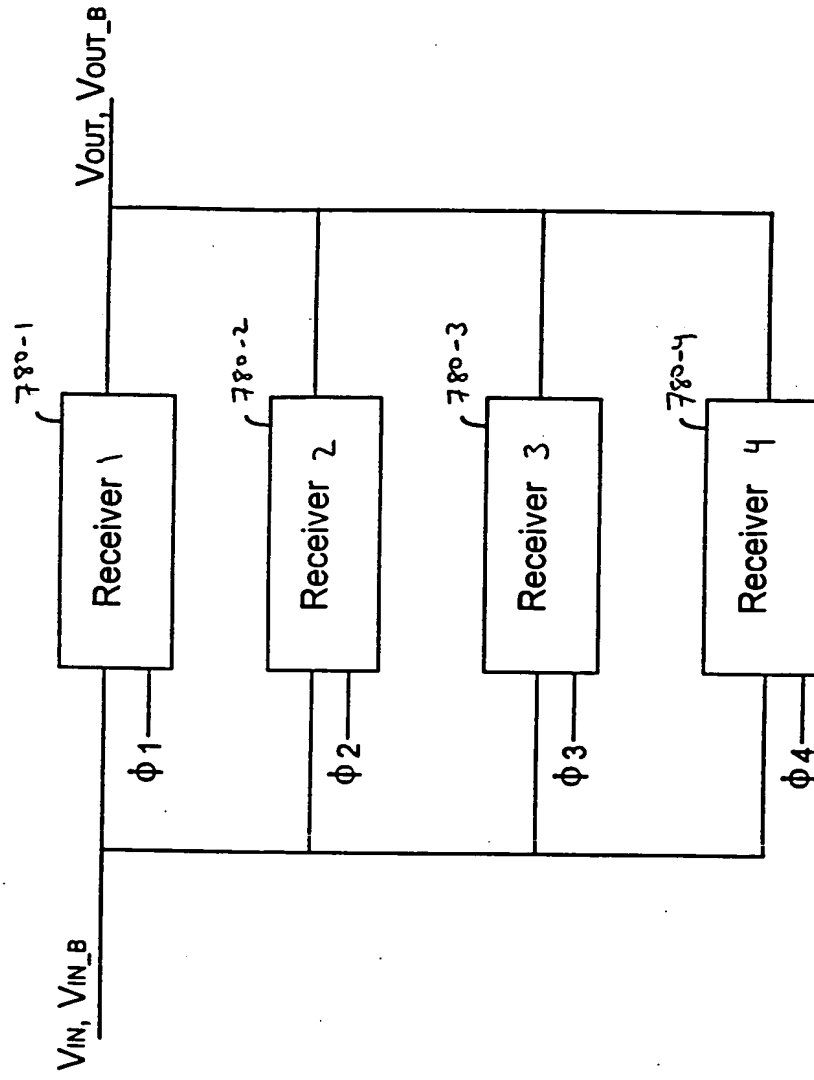
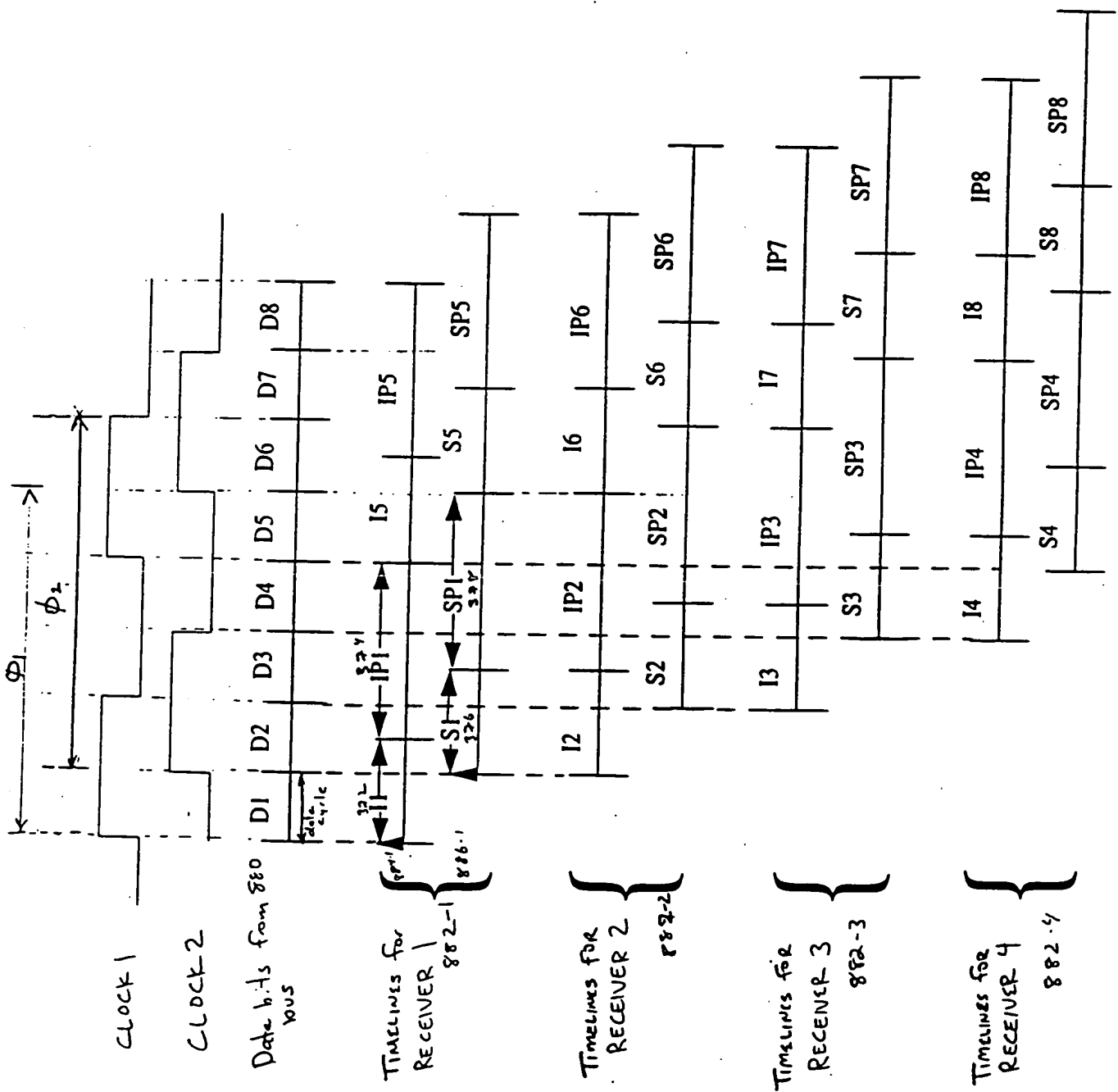


FIG 24



time

FIG. 25

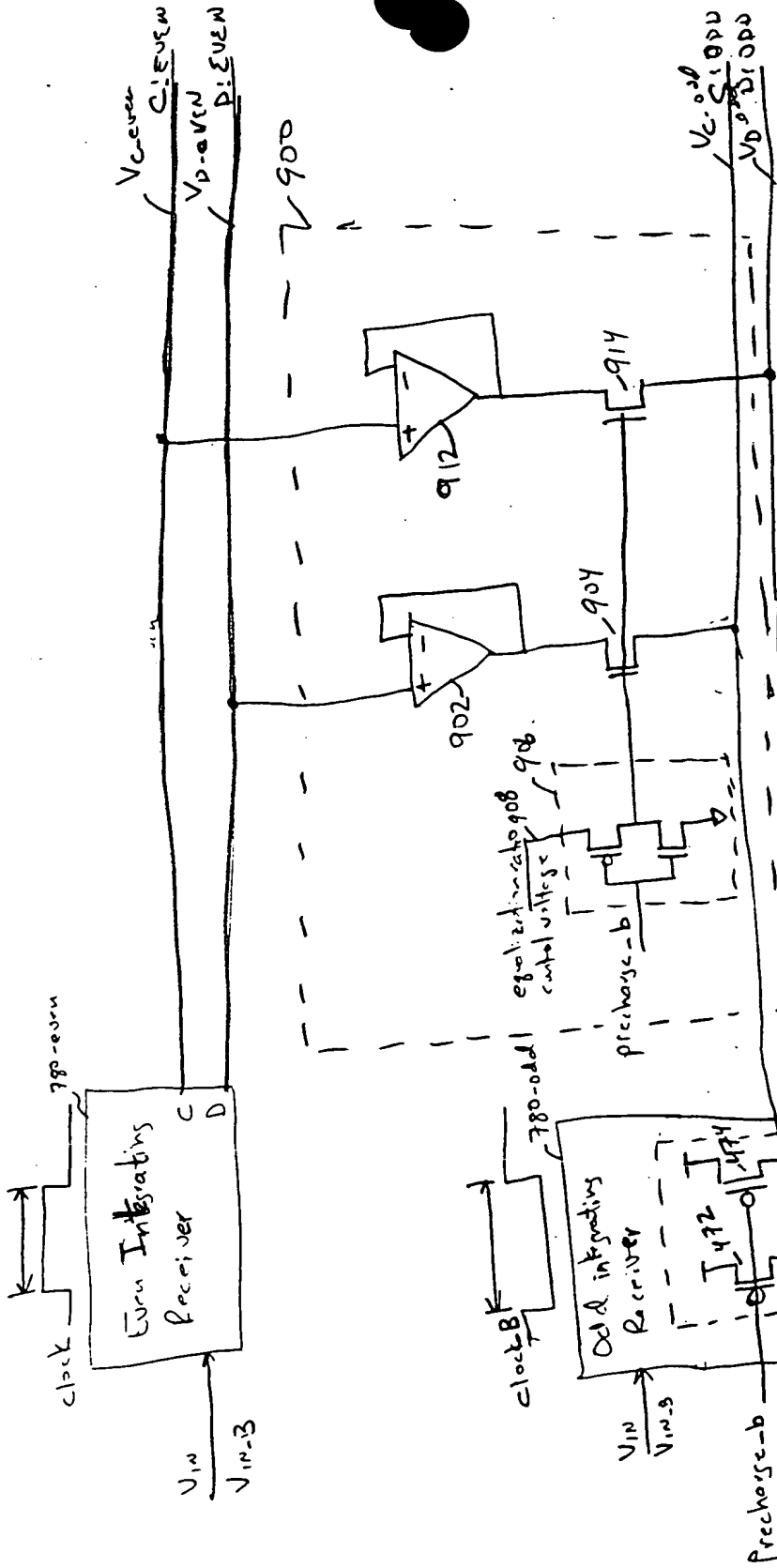


FIG. 26A

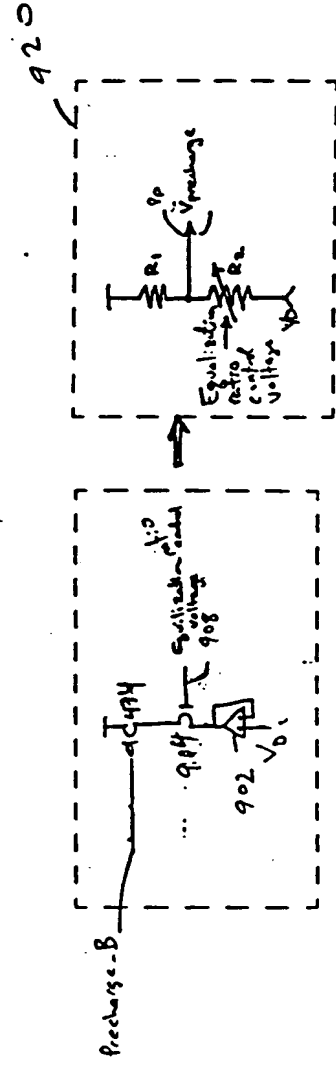


FIG. 26B

FIG. 26C

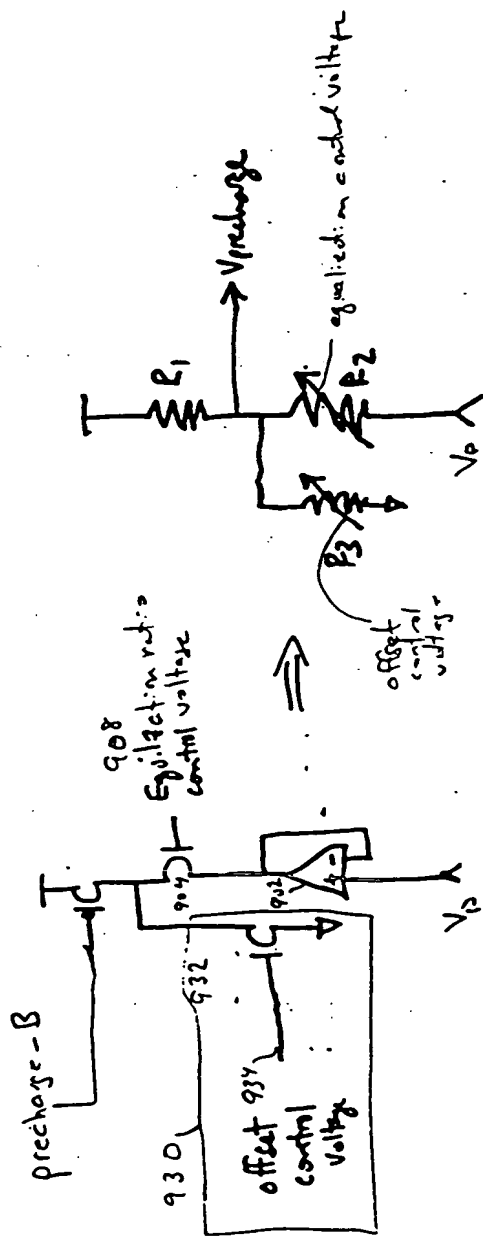
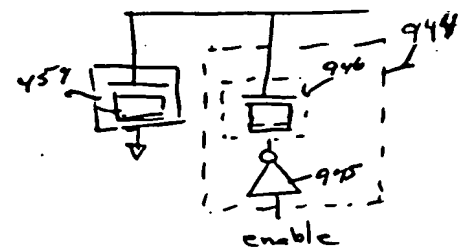
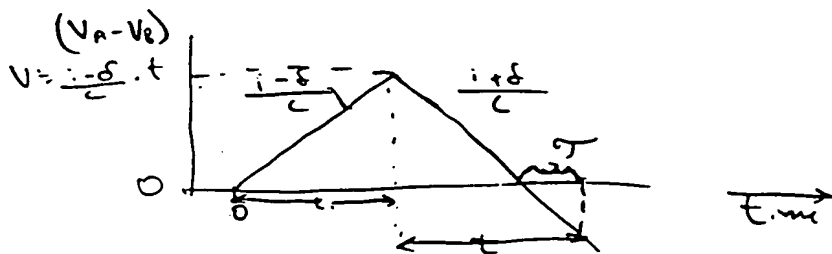
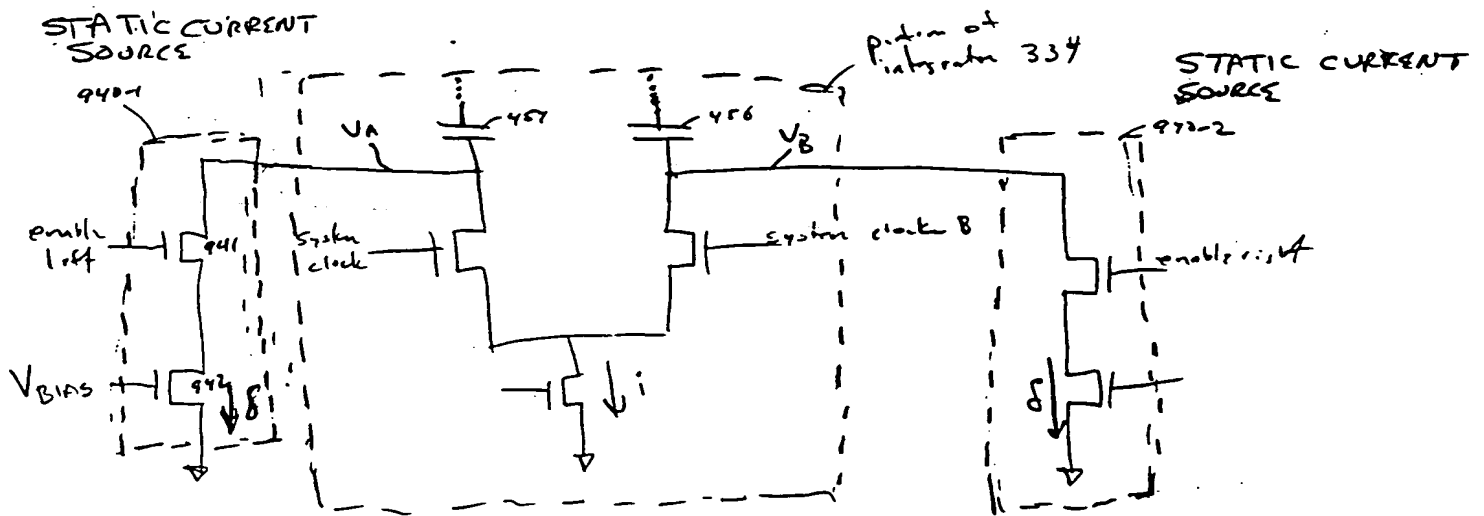
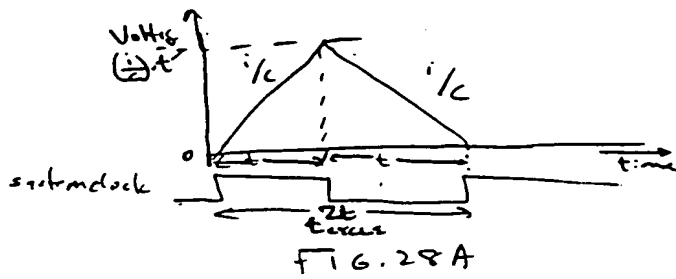


FIG. 27B

FIG. 27A



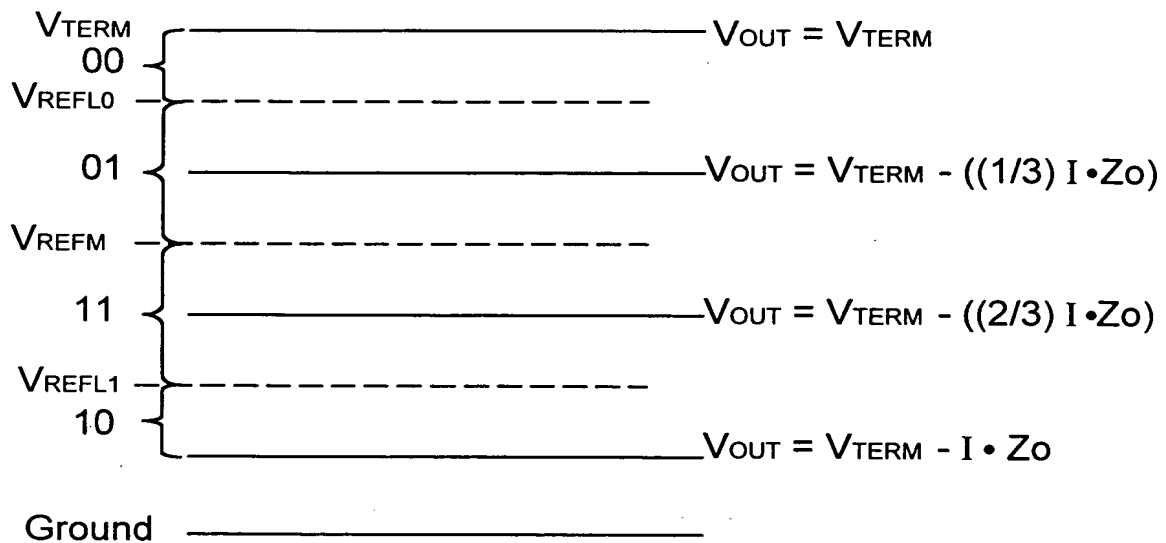


FIG. 29

005070-9168460

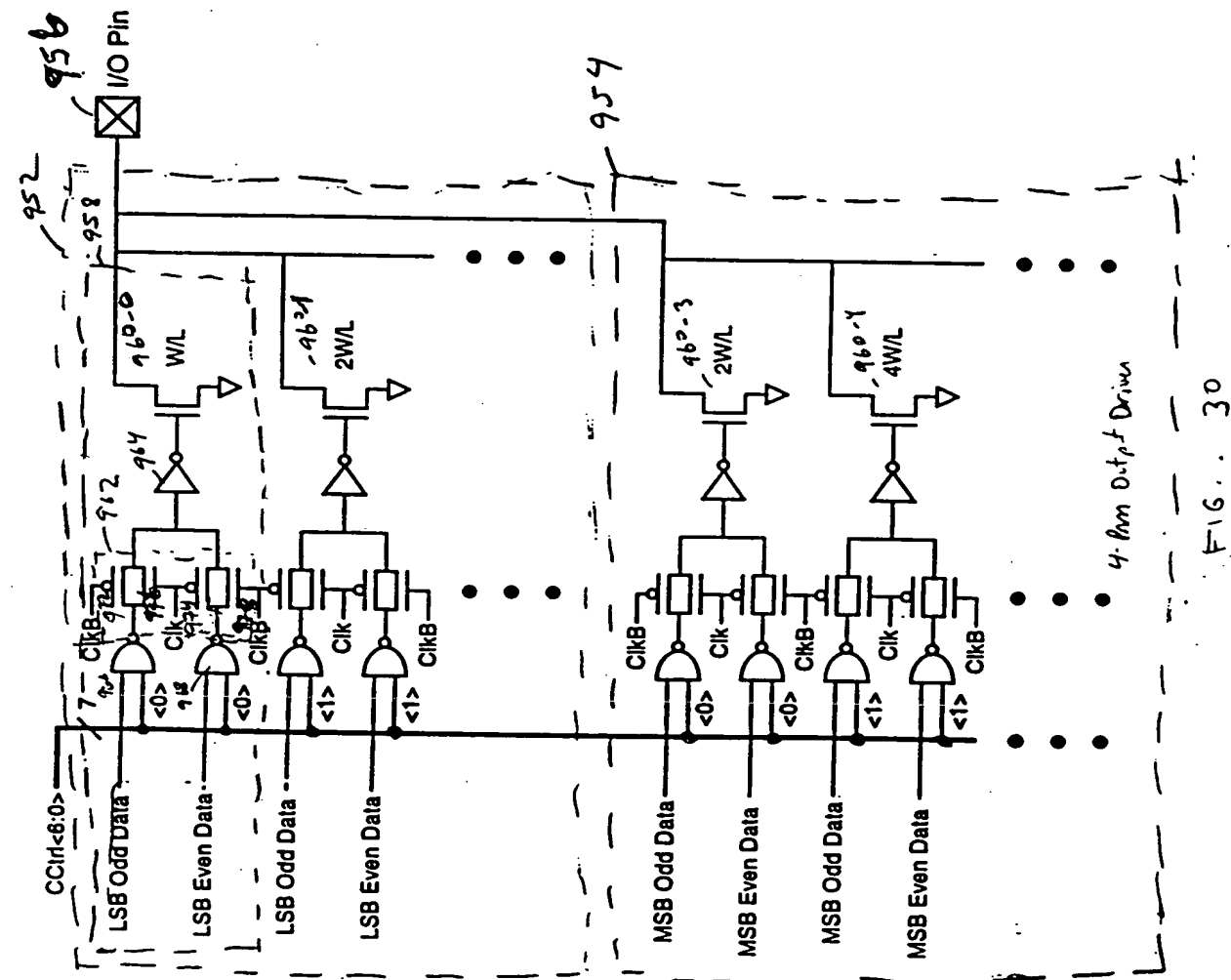


FIG. 30

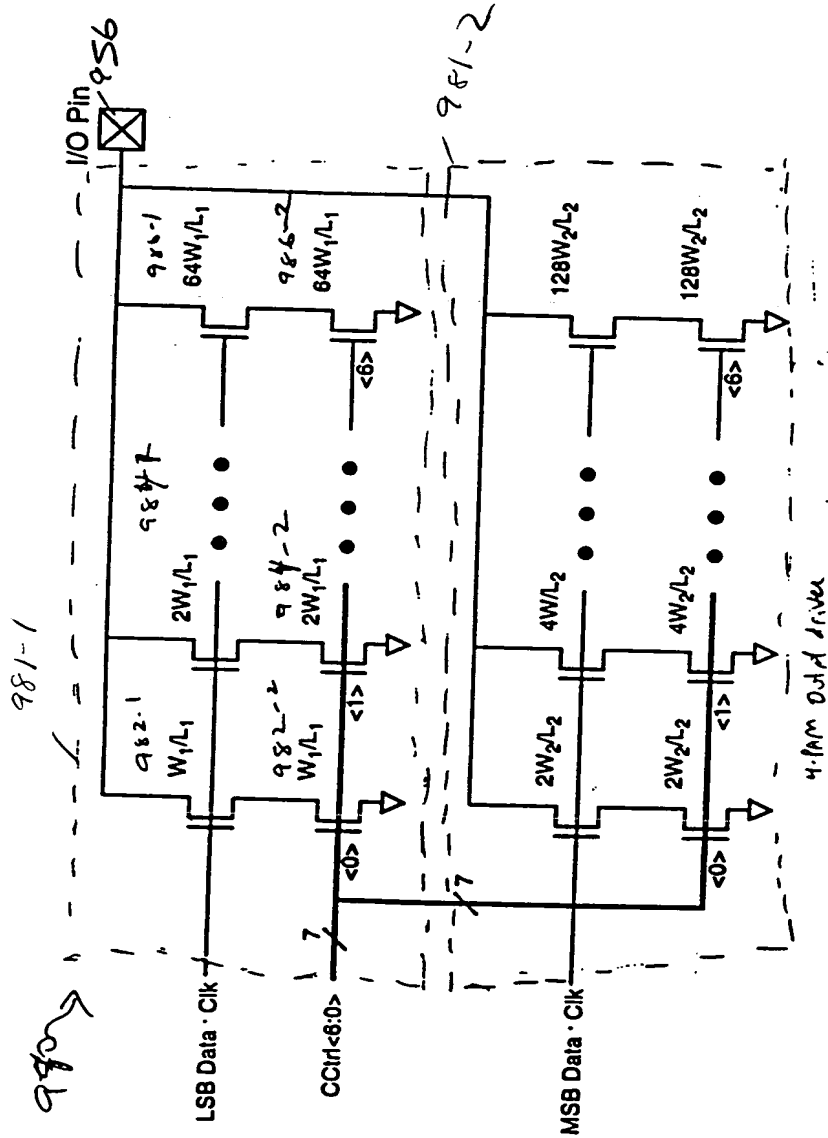


FIG. 31

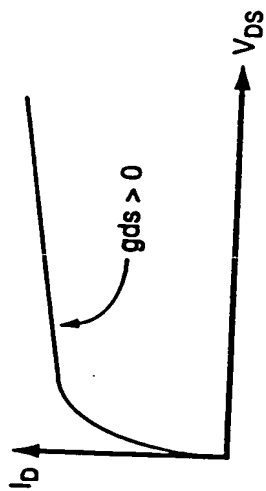


FIG. 32A

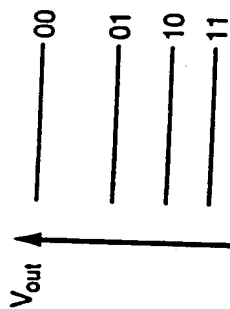


FIG. 32B

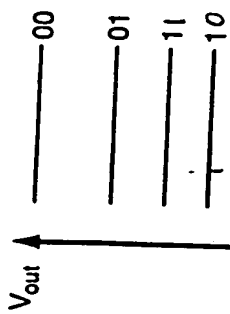


FIG. 32C

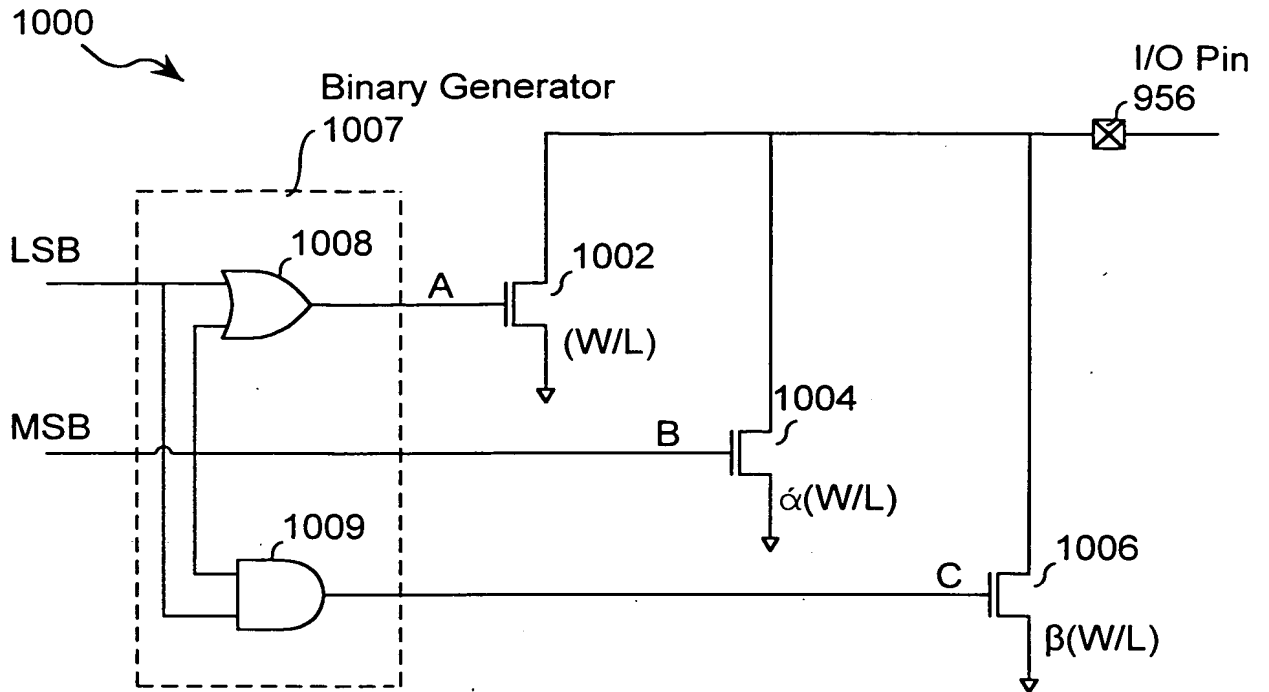
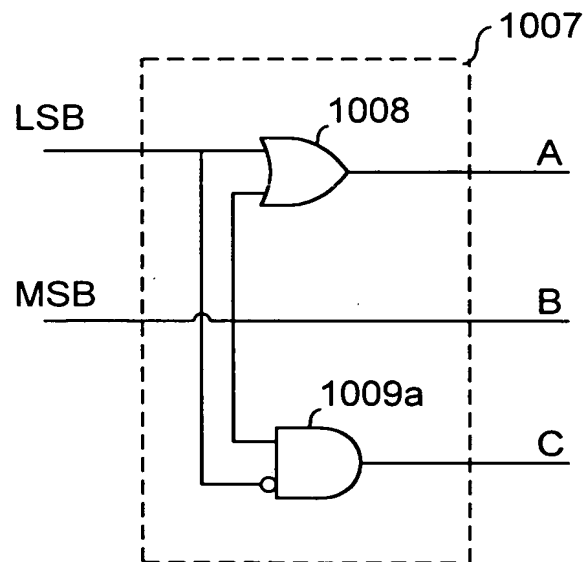
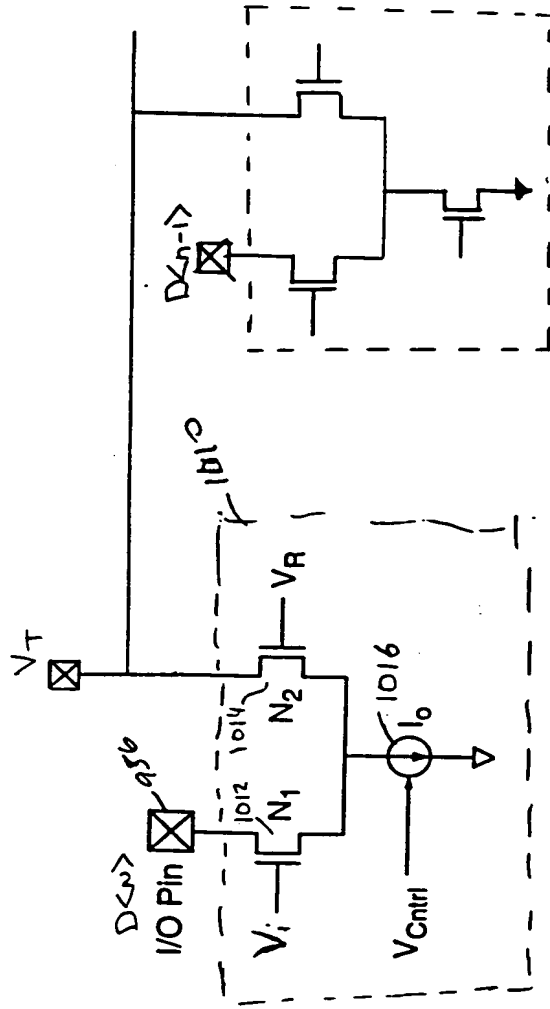


FIG. 33A



Gray Code Generator

FIG. 33B



Circuit to Reduce Switching Noise

FIG. 34

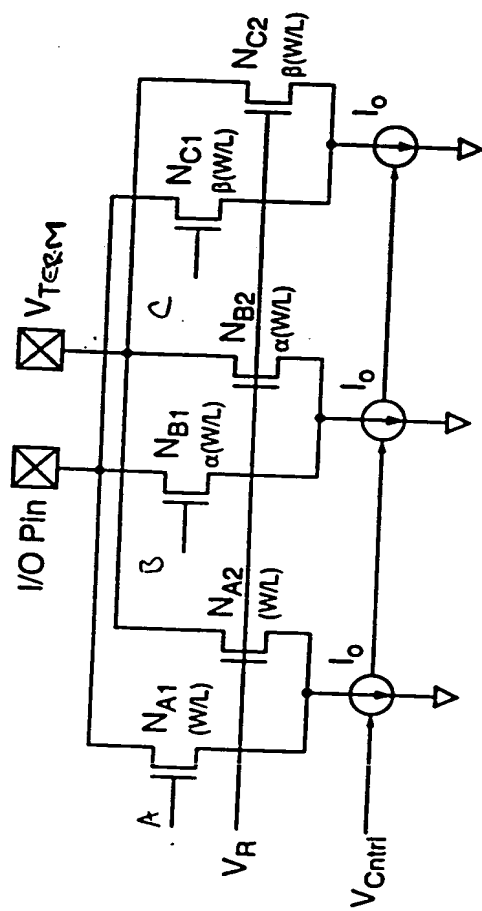
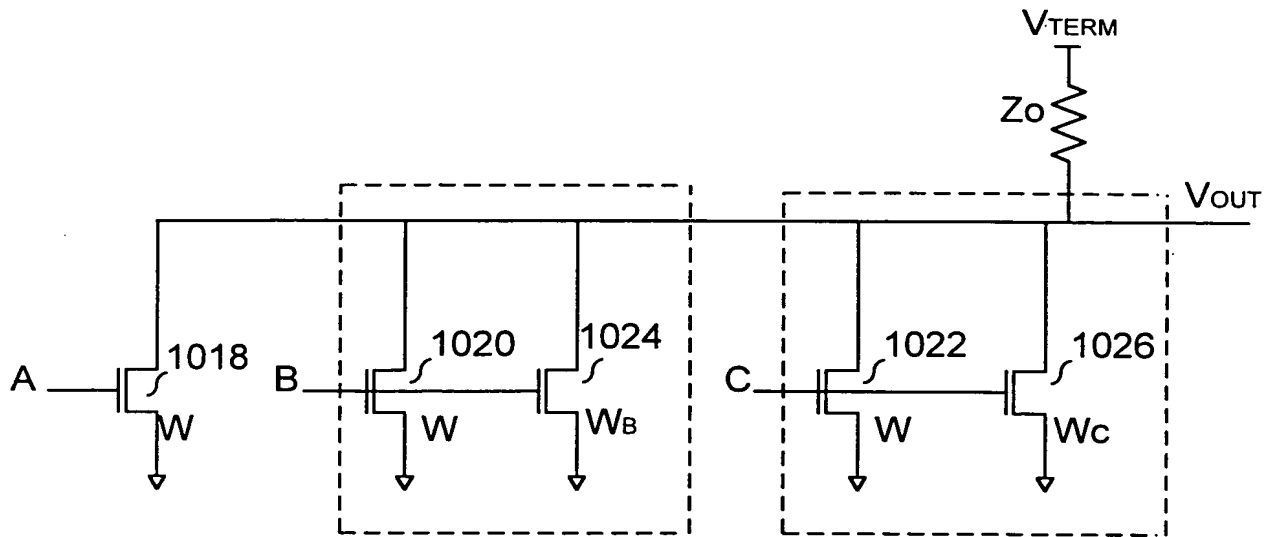
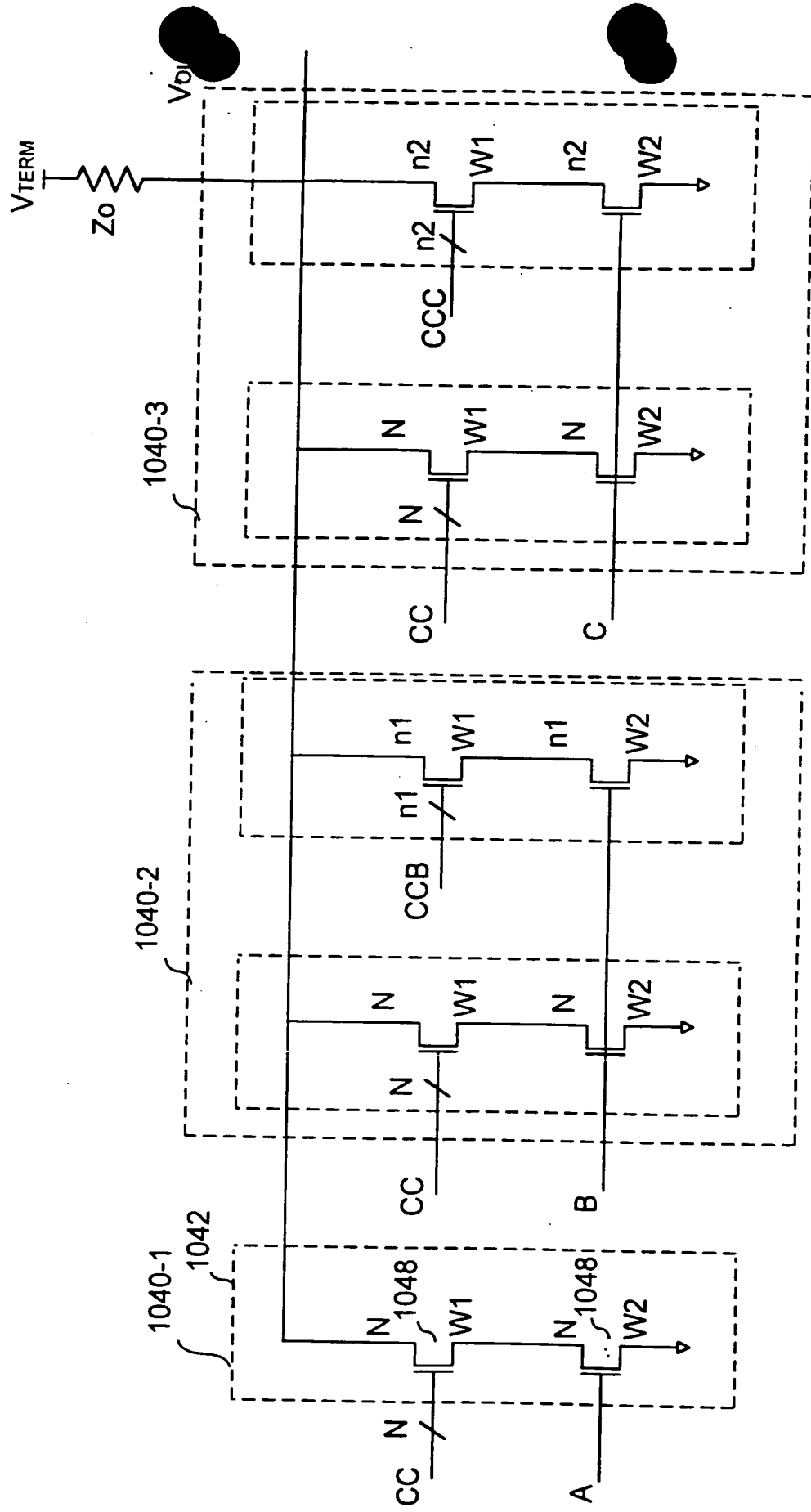


FIG. 35



GDS Compensated Multi-PAM Output Driver
FIG. 36



GDS Compensated Multi-PAM Output Driver with Current Control
FIG. 37A

1042 ↗

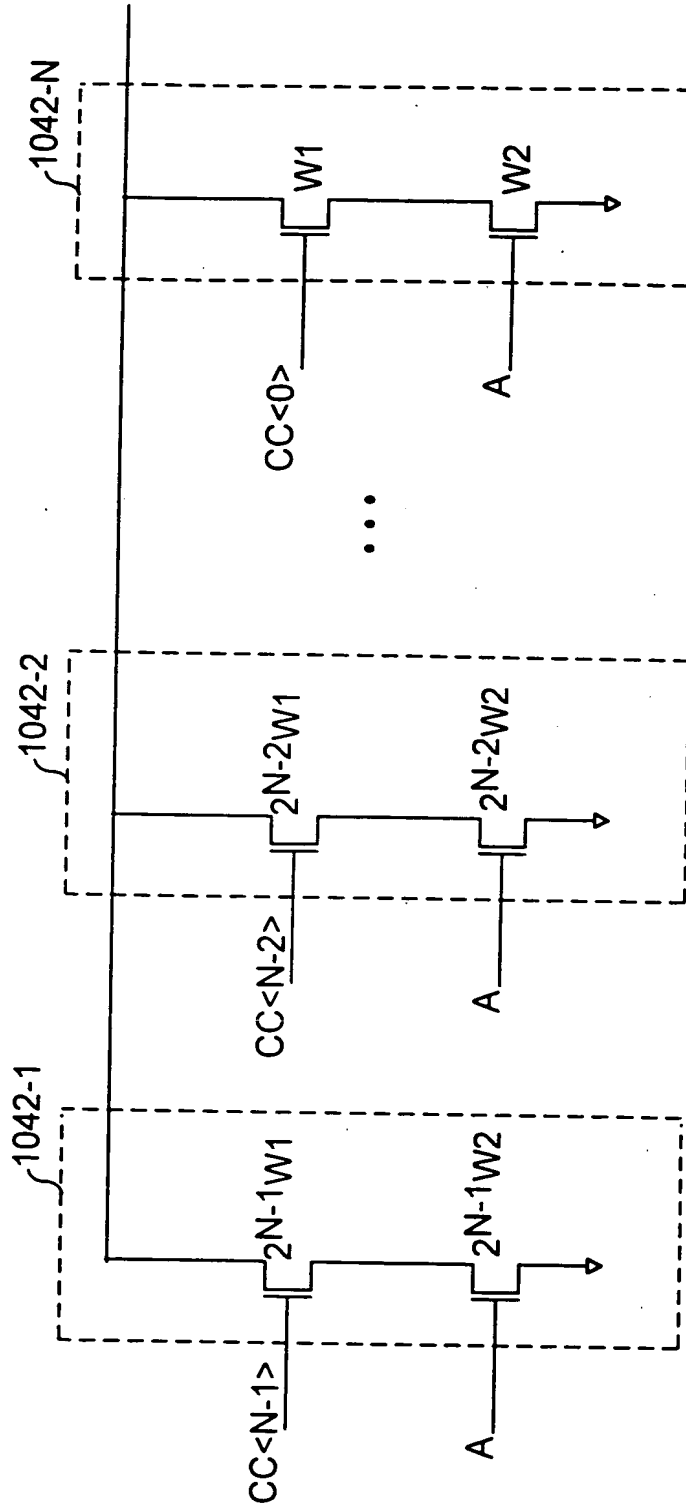
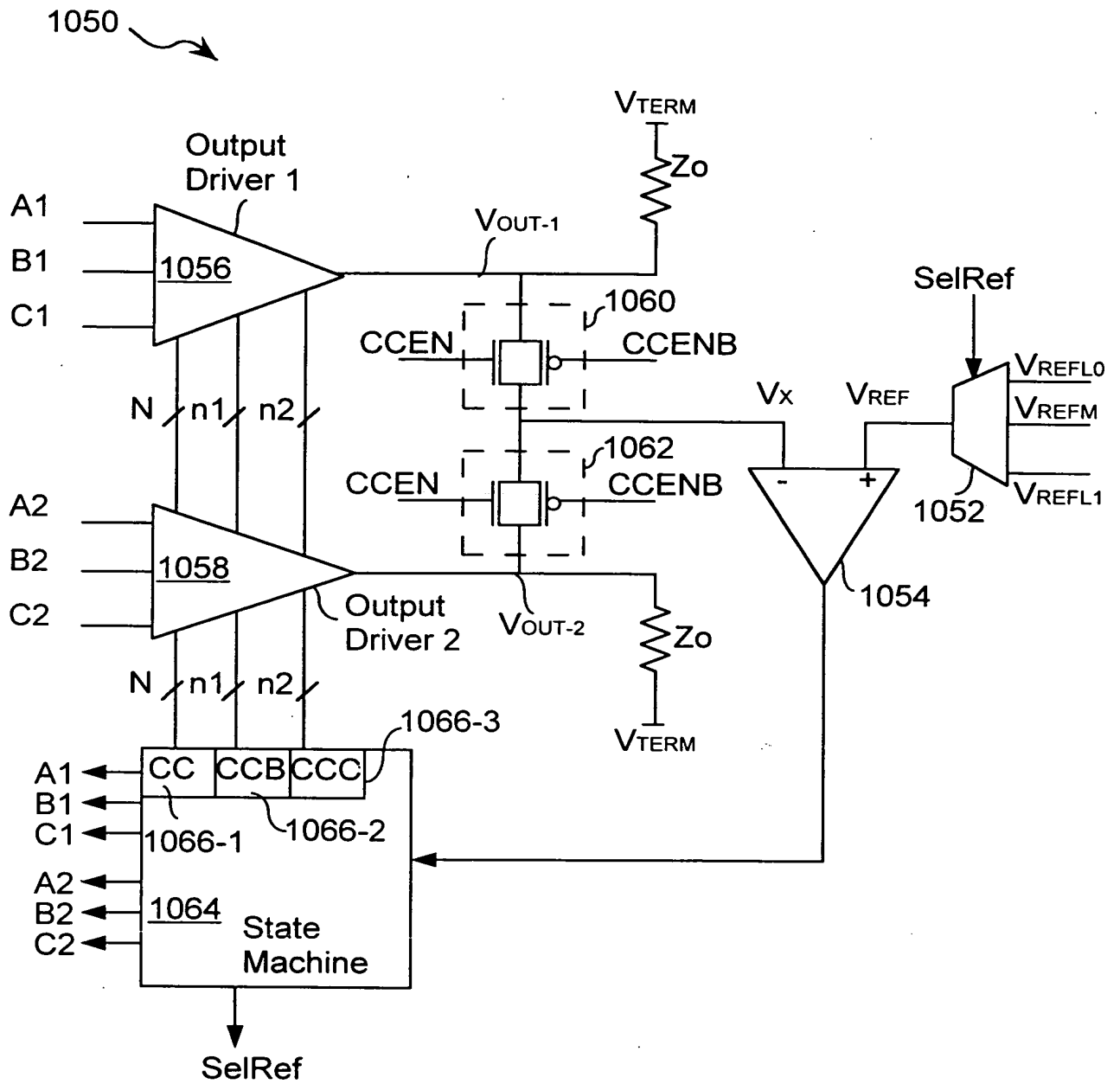


FIG. 37B



Circuit for Calibrating the GDS Compensated Output Driver
with Current Control

FIG. 38

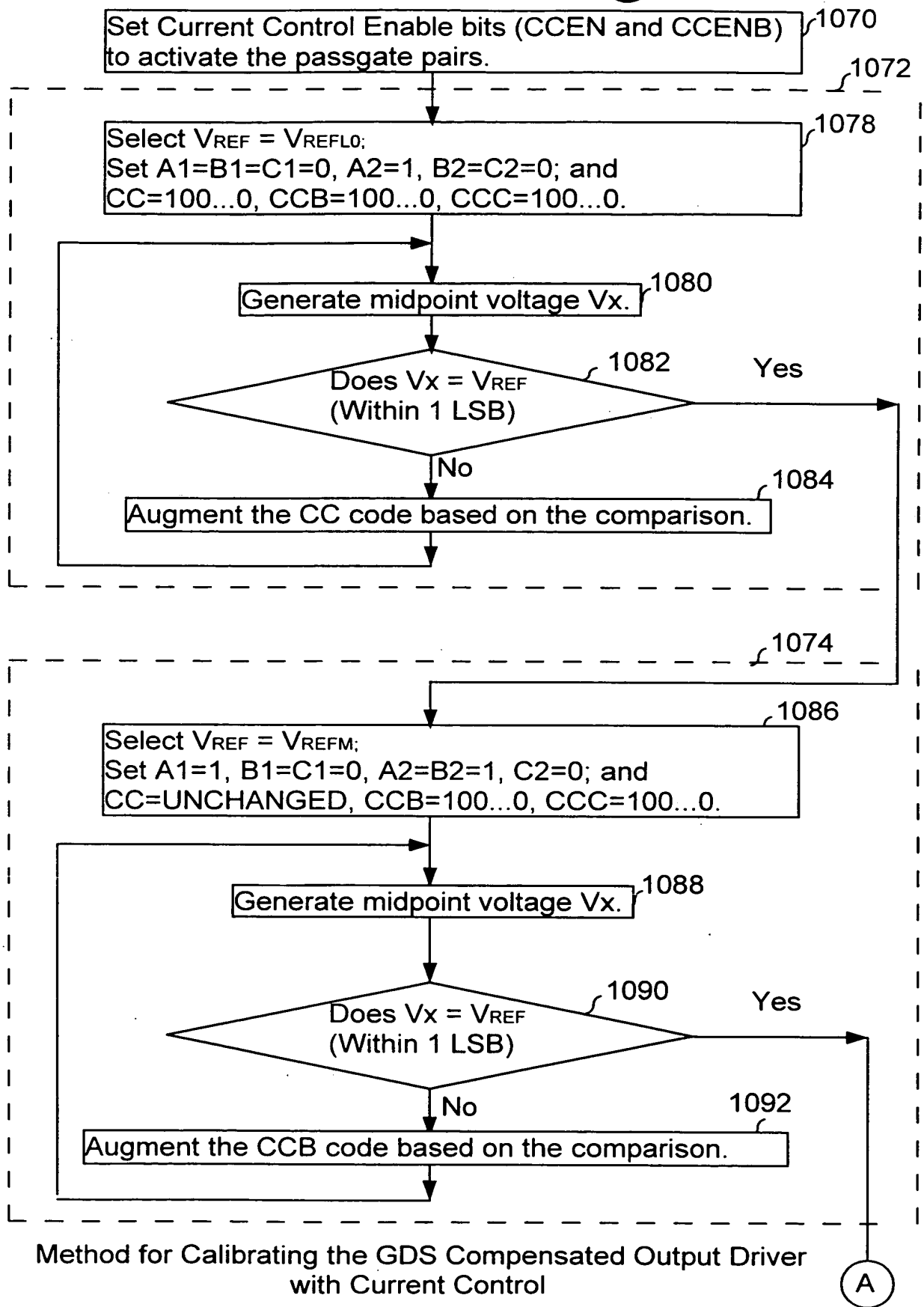
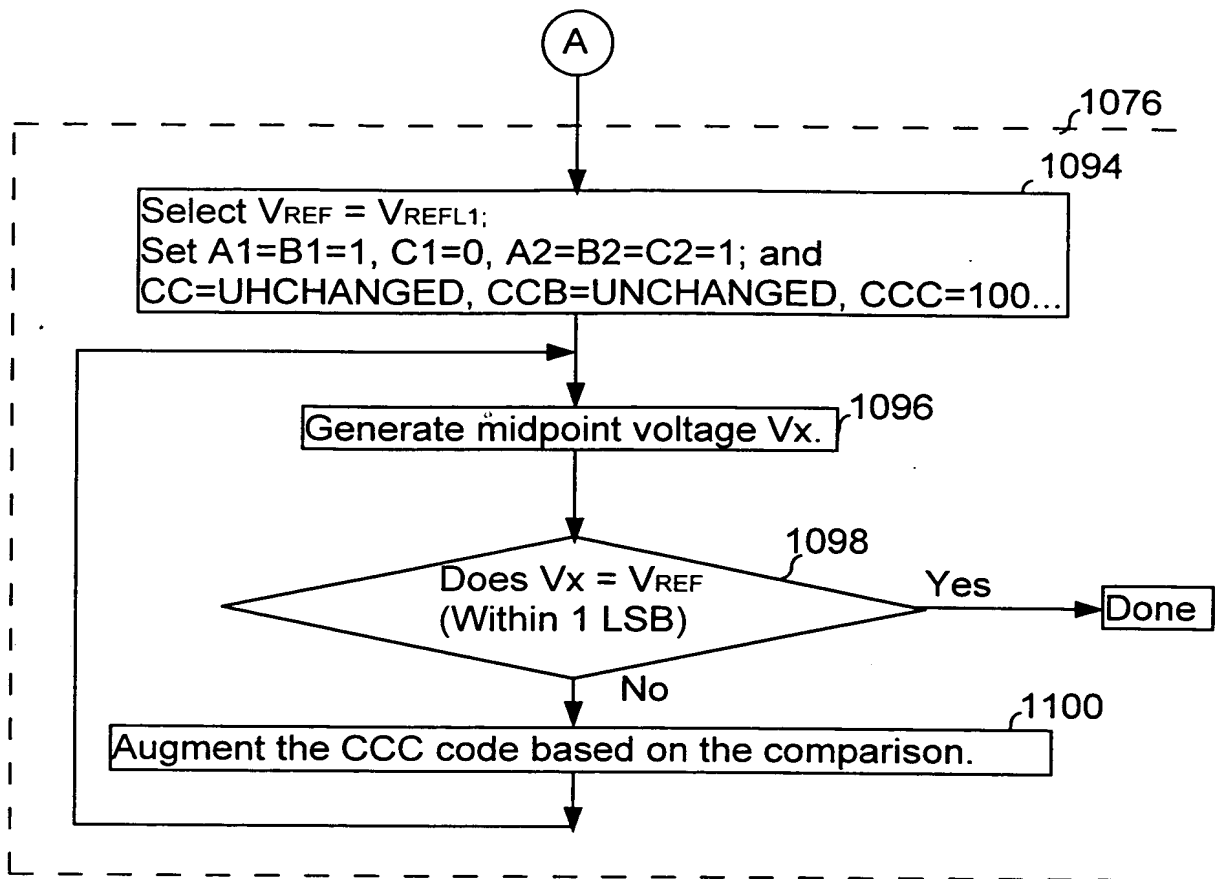
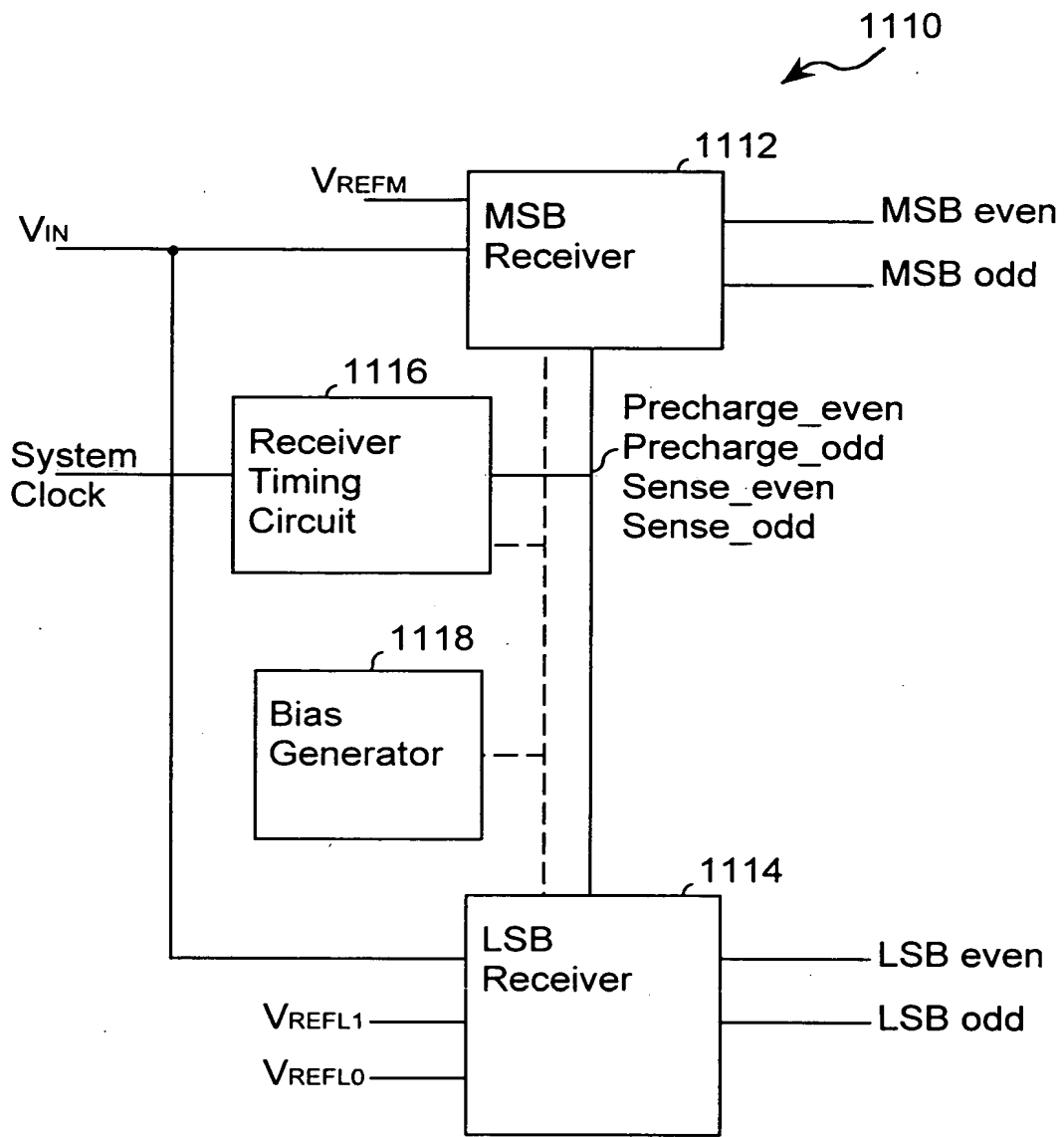


FIG. 39A



Method for Calibrating the GDS Compensated Output Driver
with Current Control

FIG. 39B



Multi-PAM Receiver
FIG. 40

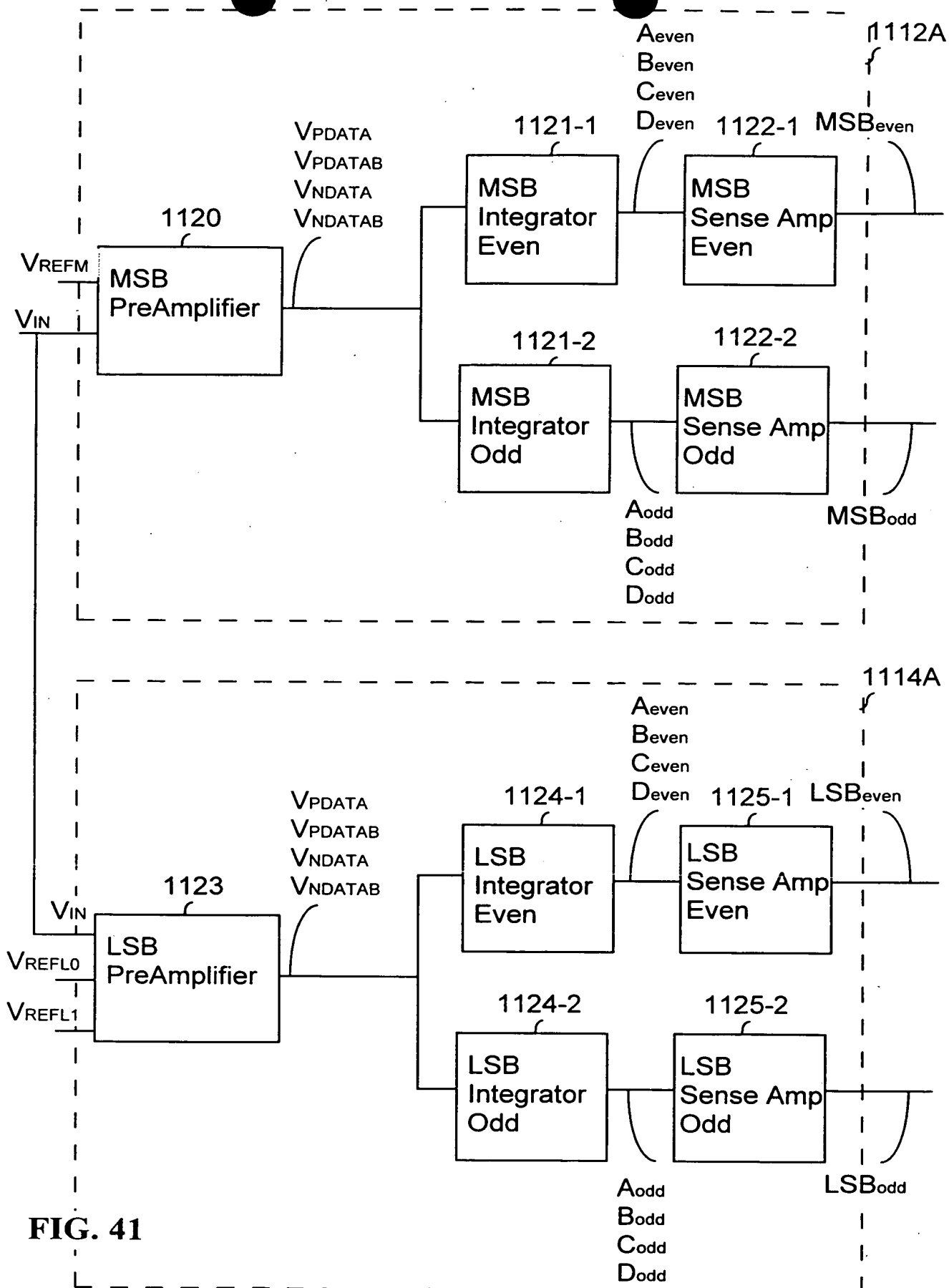


FIG. 41

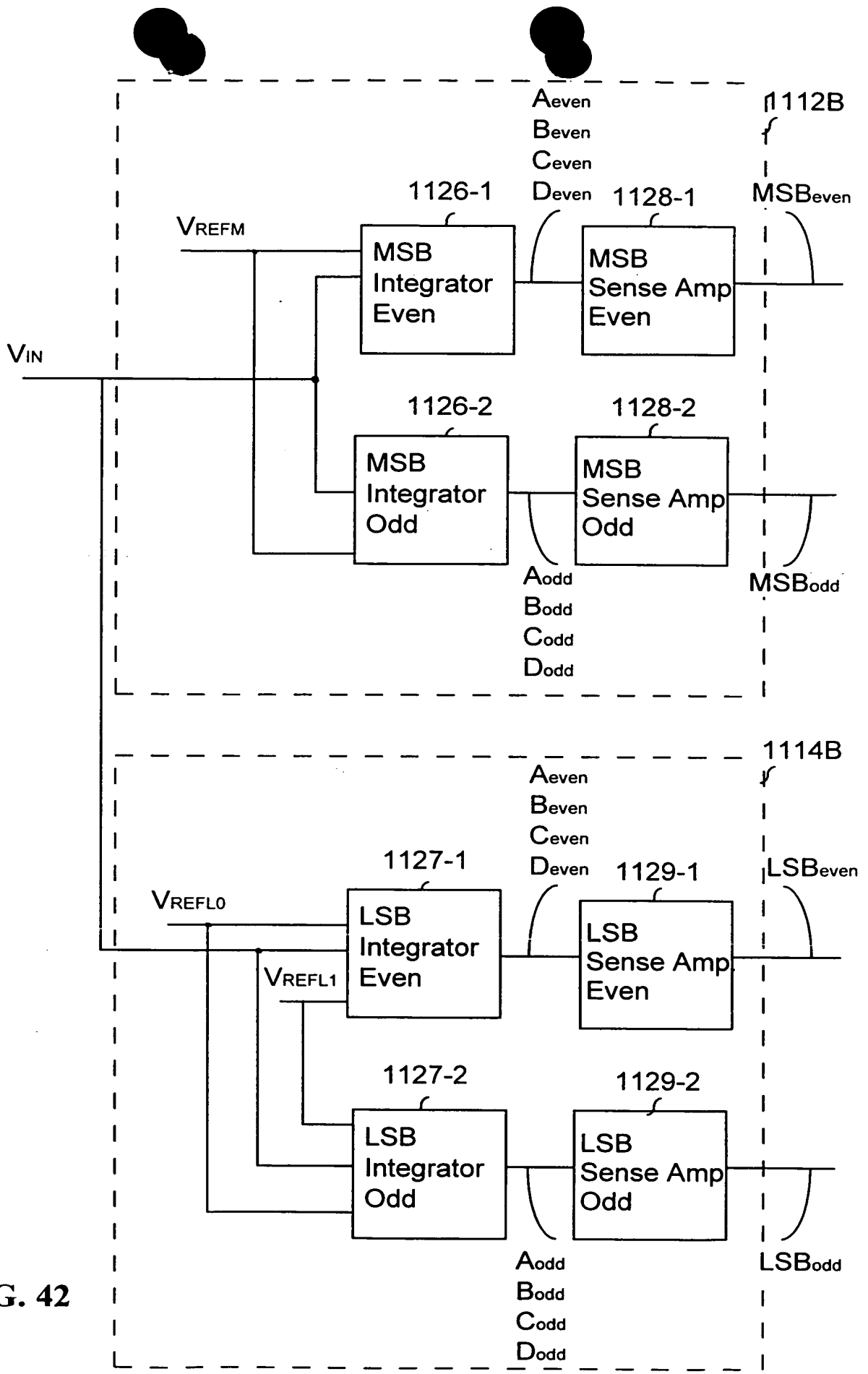
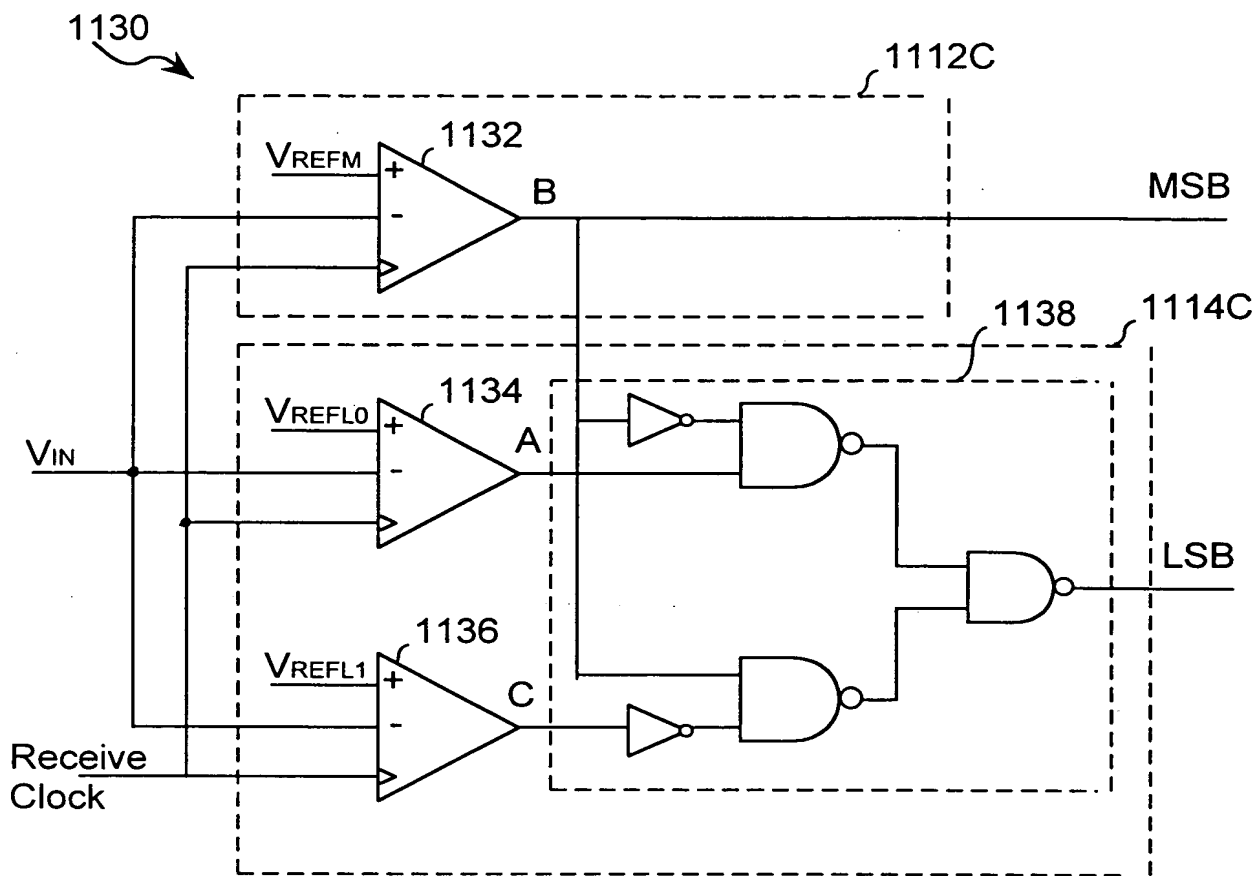


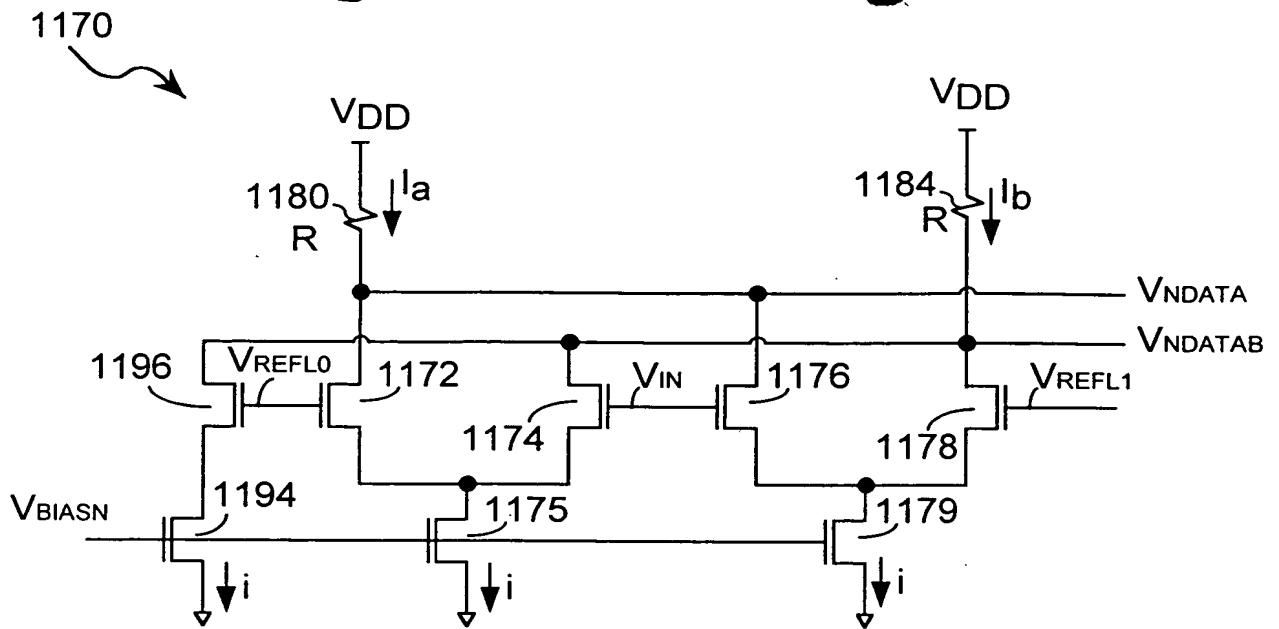
FIG. 42

MULTI-PAM RECEIVER

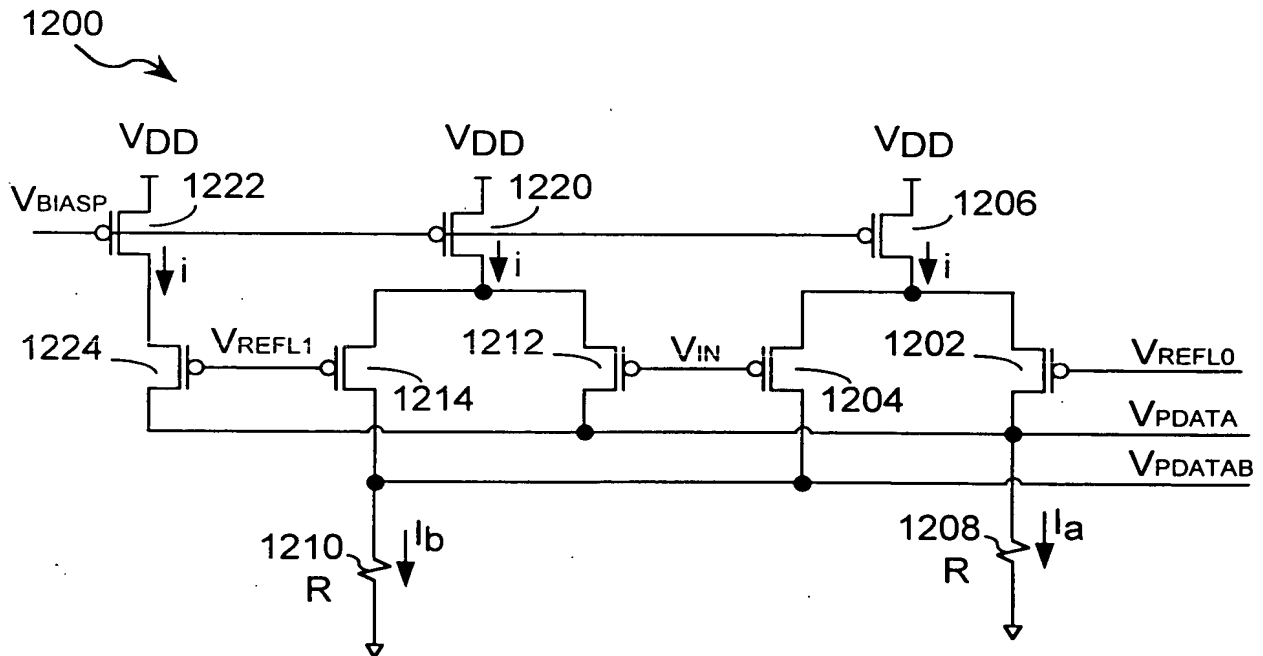


Multi-PAM Receiver
FIG. 43

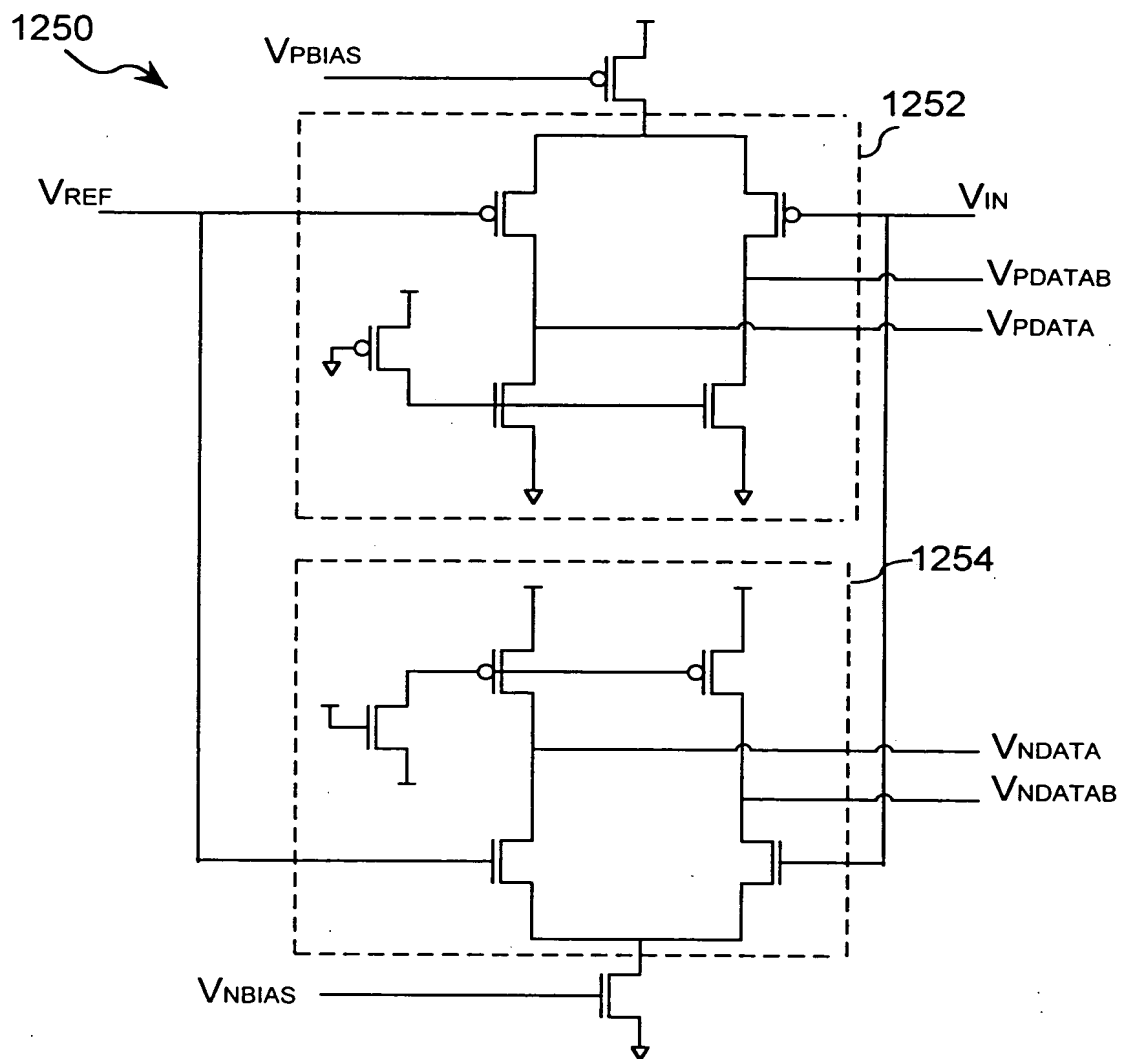
FIG. 44



Multi-PAM Pre-Amplifier
FIG. 45A



Multi-PAM Pre-Amplifier
FIG. 45B



Multi-PAM Pre-Amplifier for MSB

FIG. 46

1330



FIG. 47.

RECEIVER TIMING CIRCUIT

1116

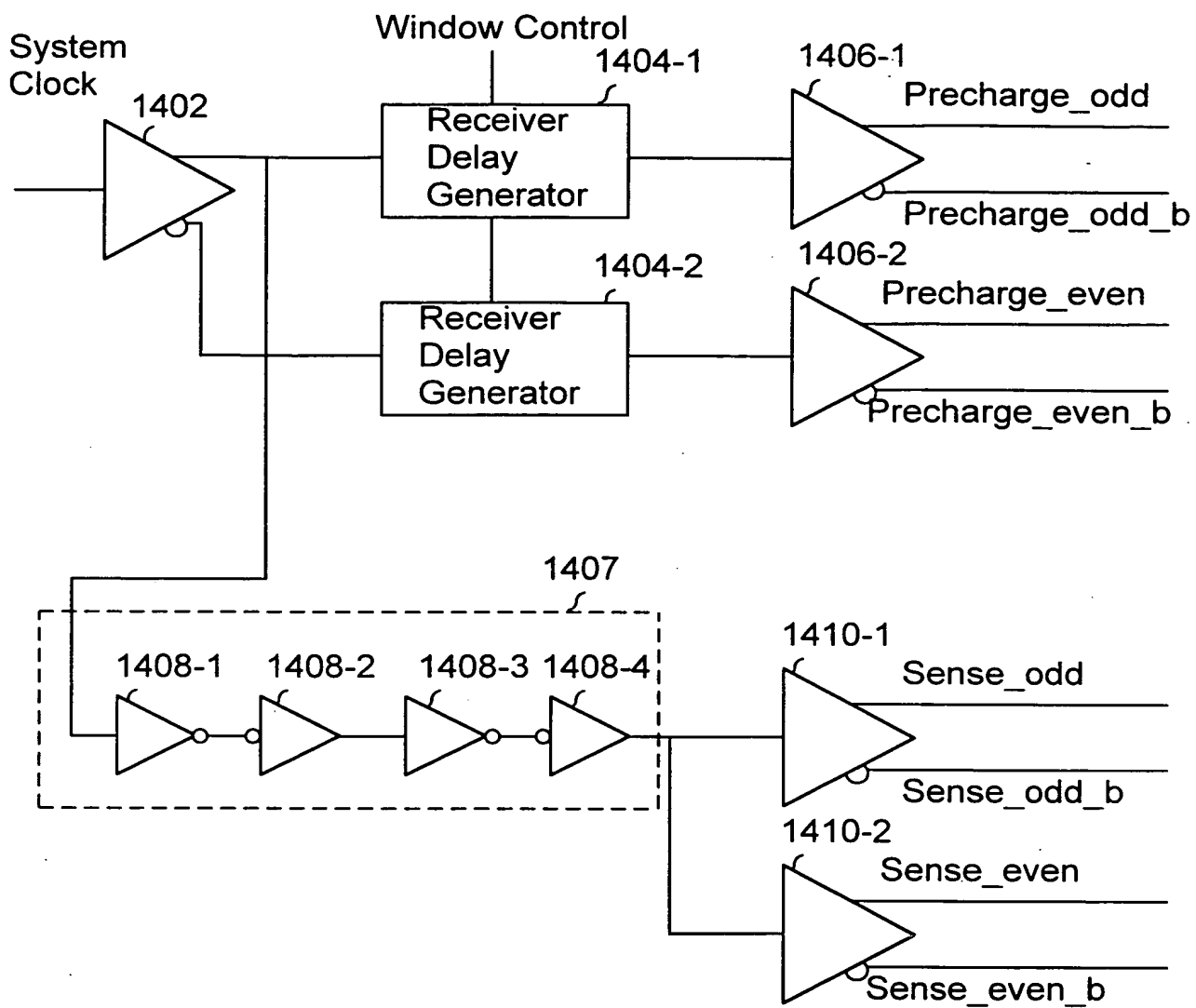
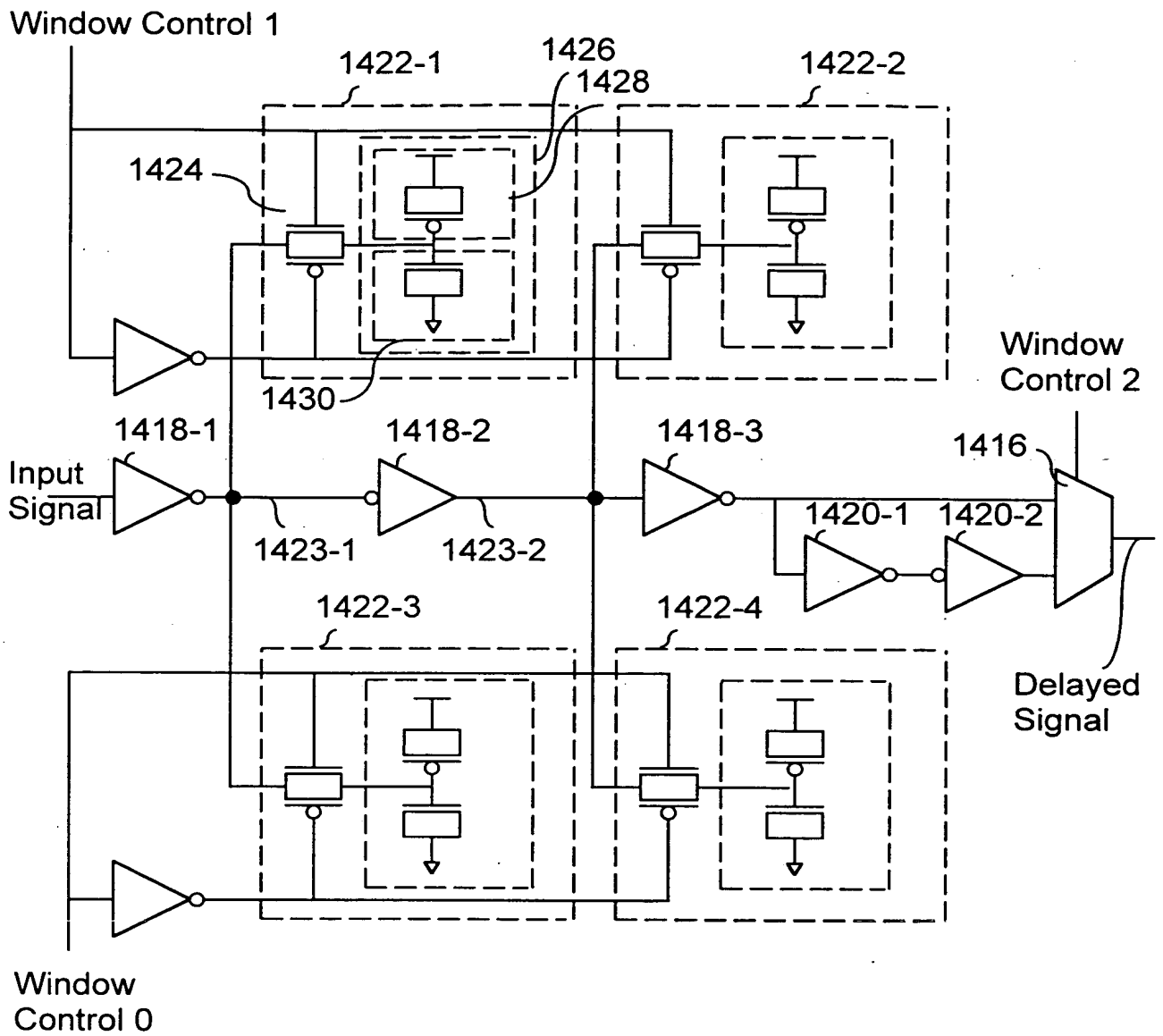


FIG. 50

1404



Receiver Delay Generator

FIG. 51

1450

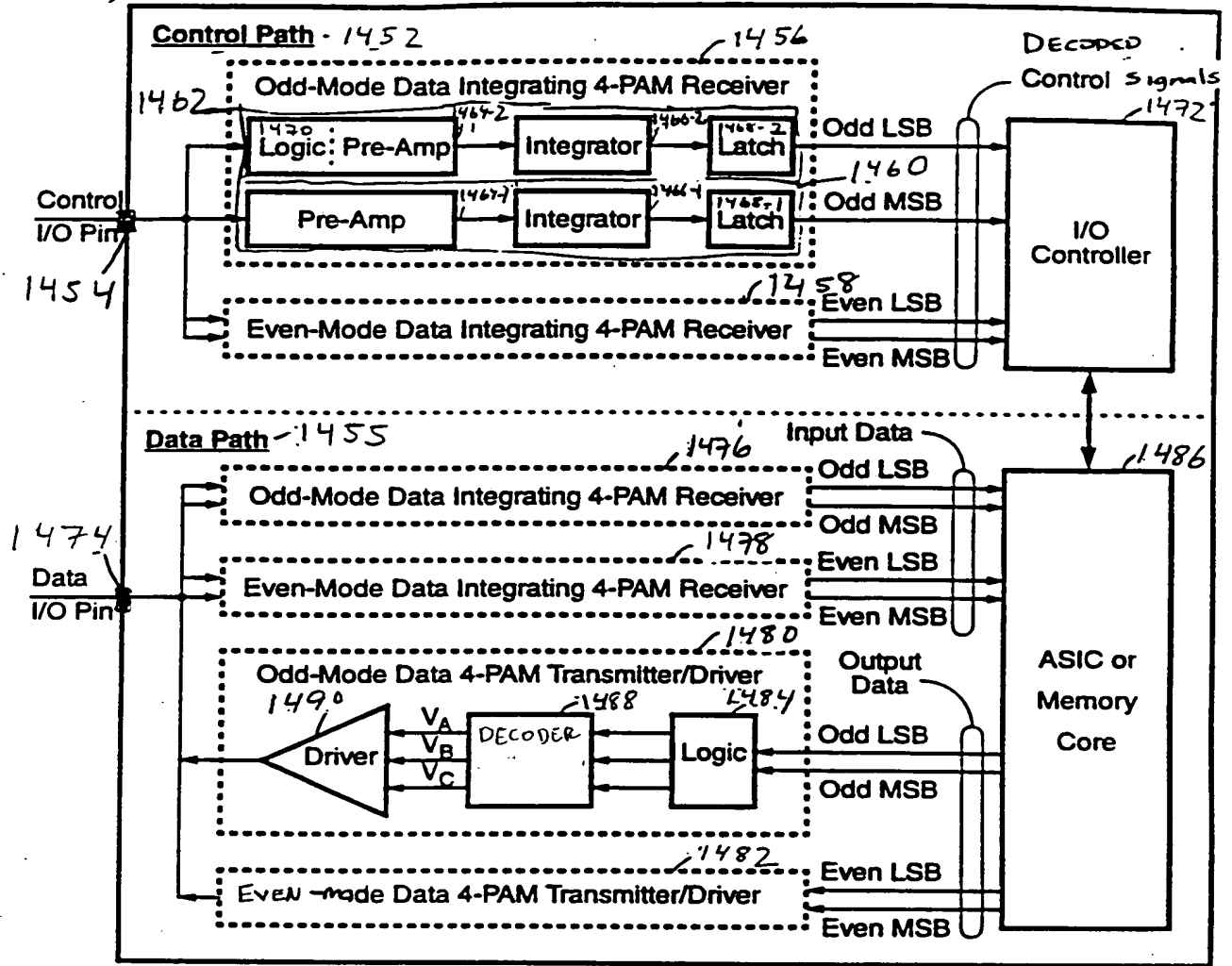
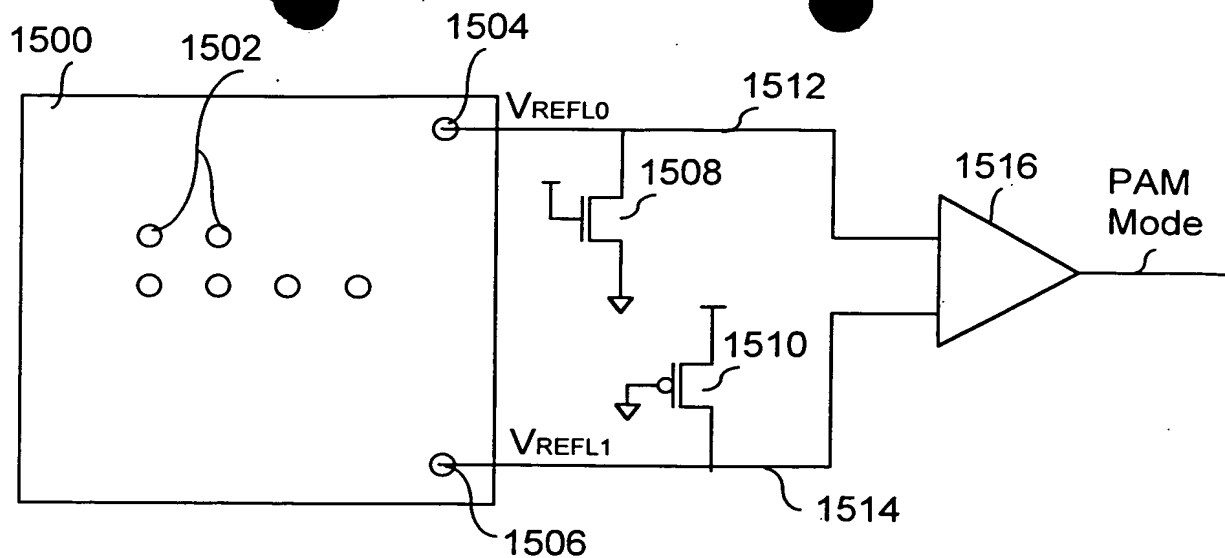


FIG. 52A

FIG. 52B



Automatic Detection of 2-PAM or 4-PAM Mode

FIG. 53

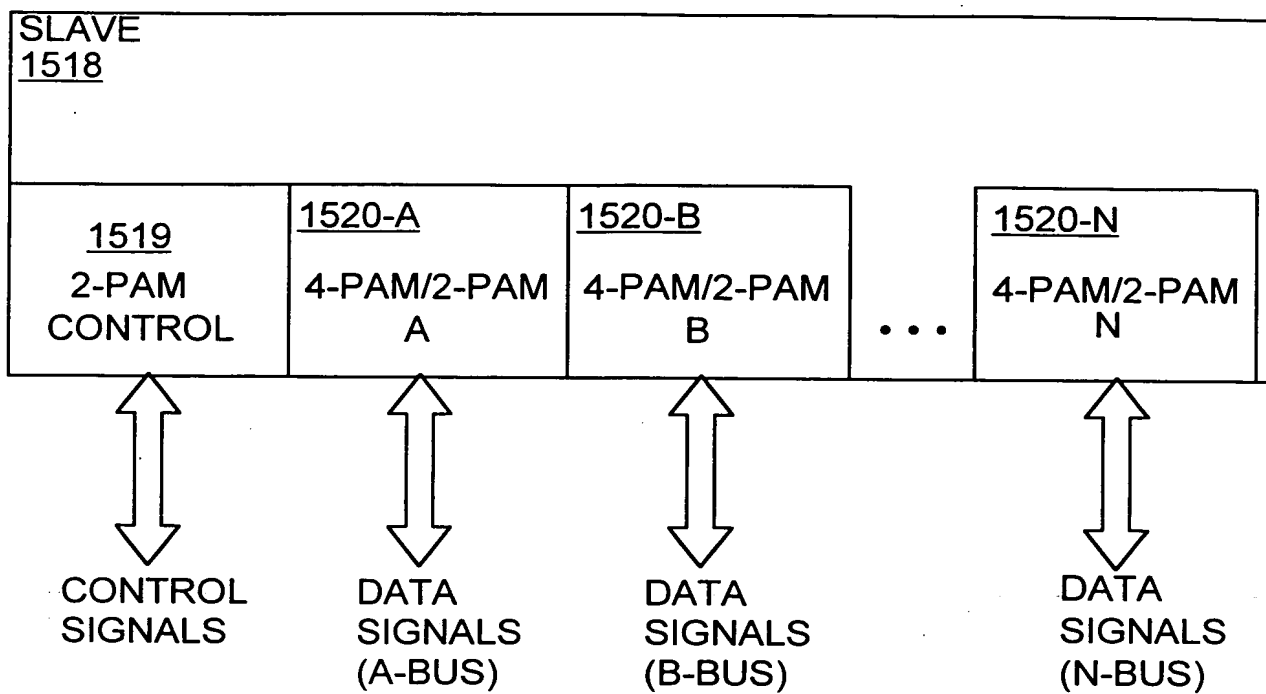


FIG. 54A

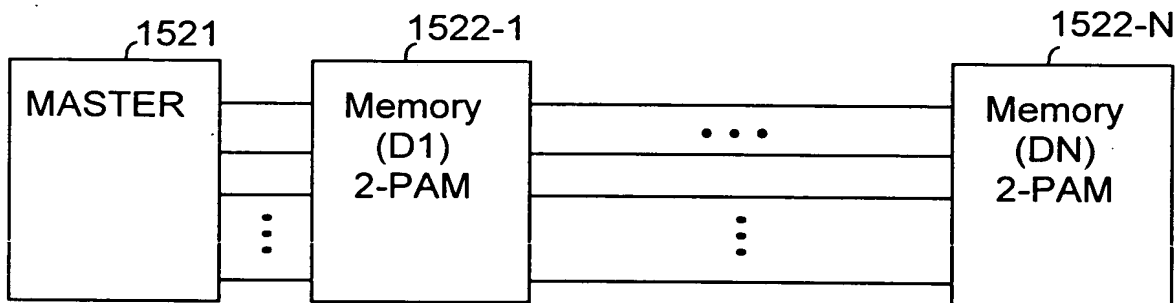


FIG. 54B

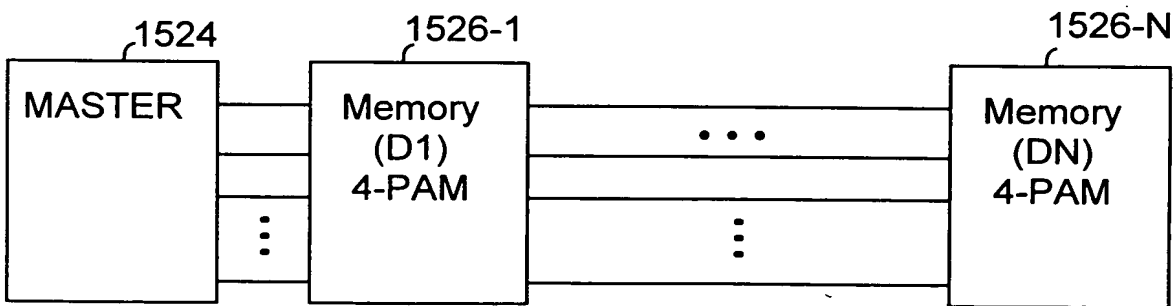
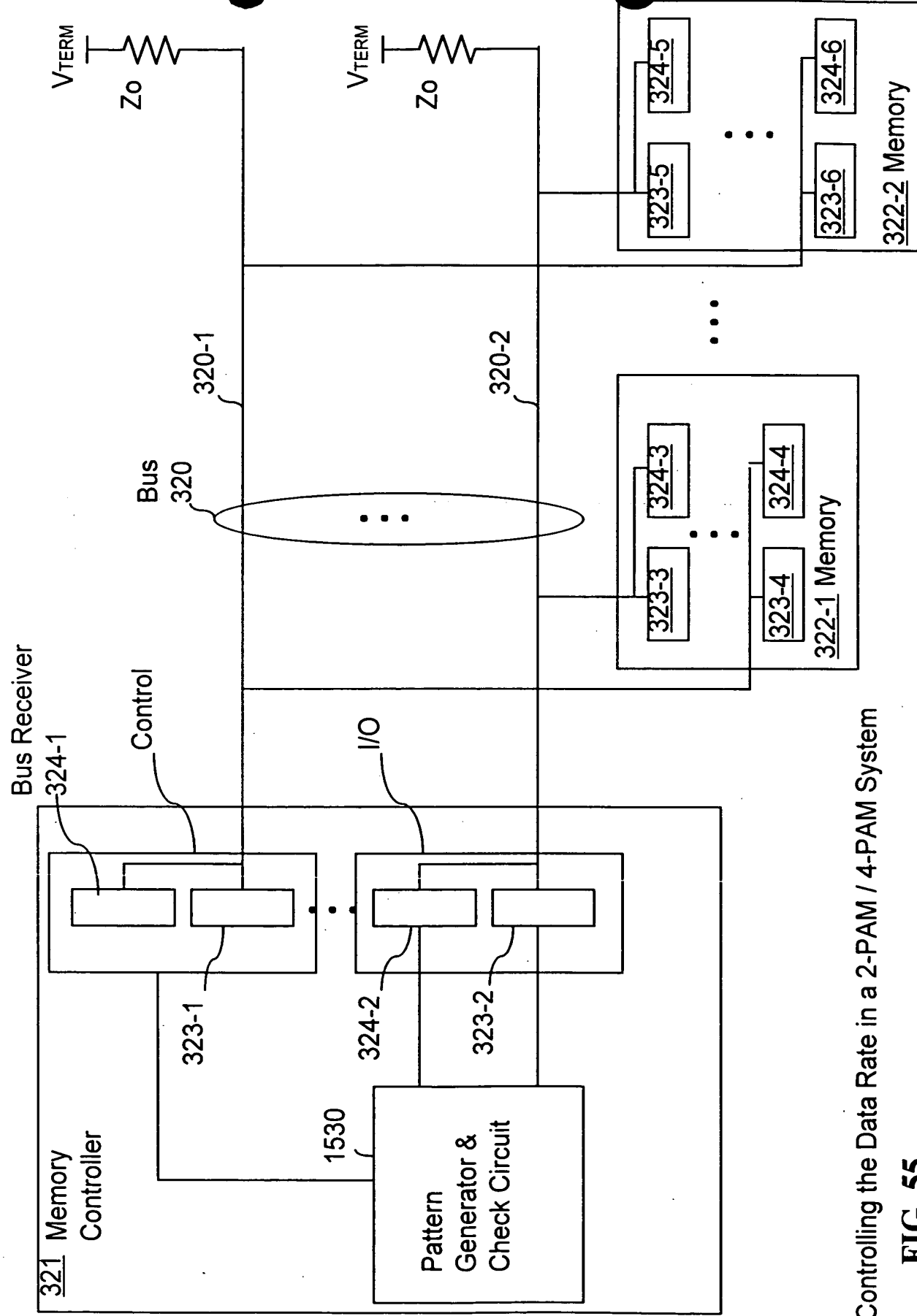
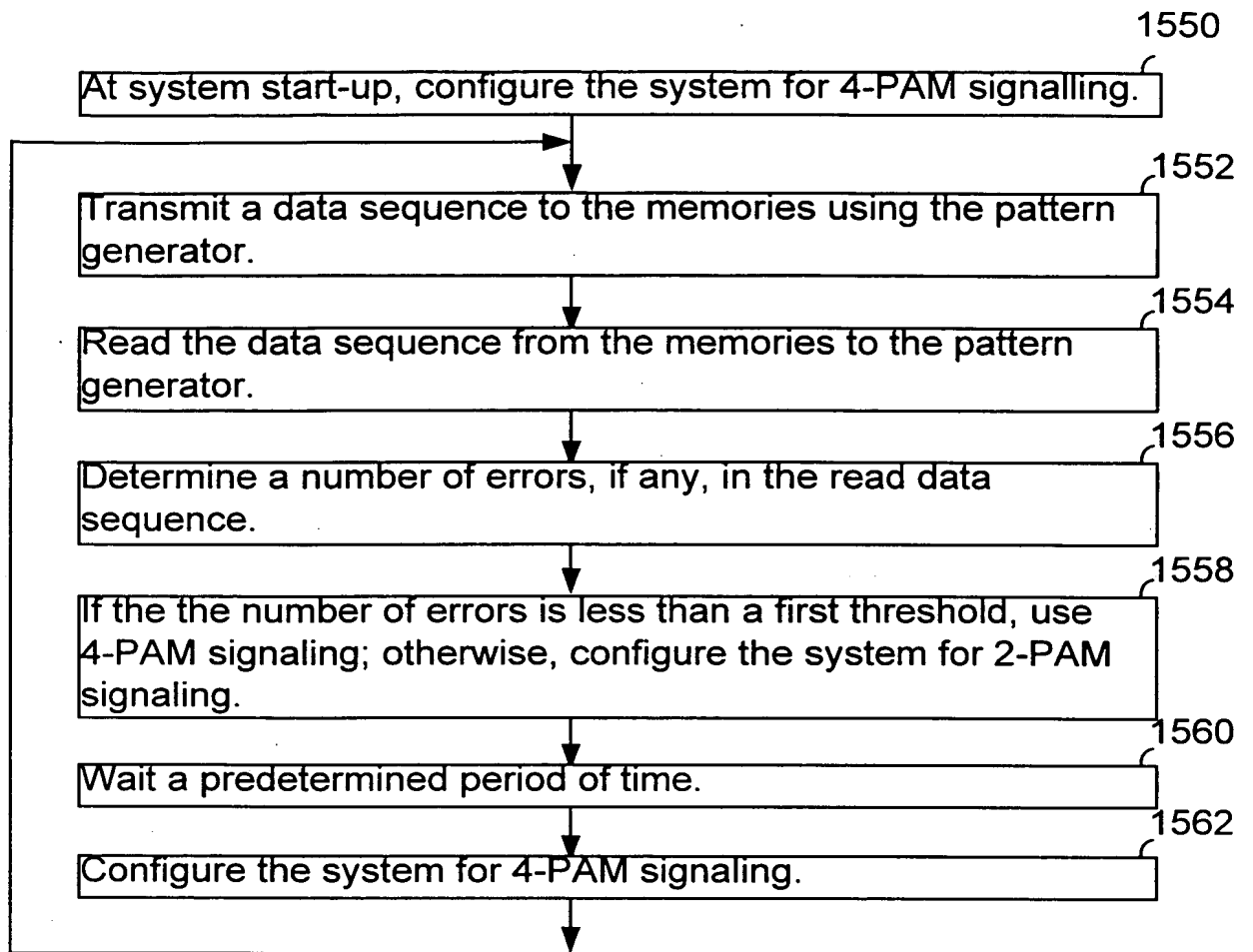


FIG. 54C



Controlling the Data Rate in a 2-PAM / 4-PAM System

FIG. 55



Method for Determining 4-PAM / 2-PAM Signalling as a
Function of Error Rate

FIG. 56

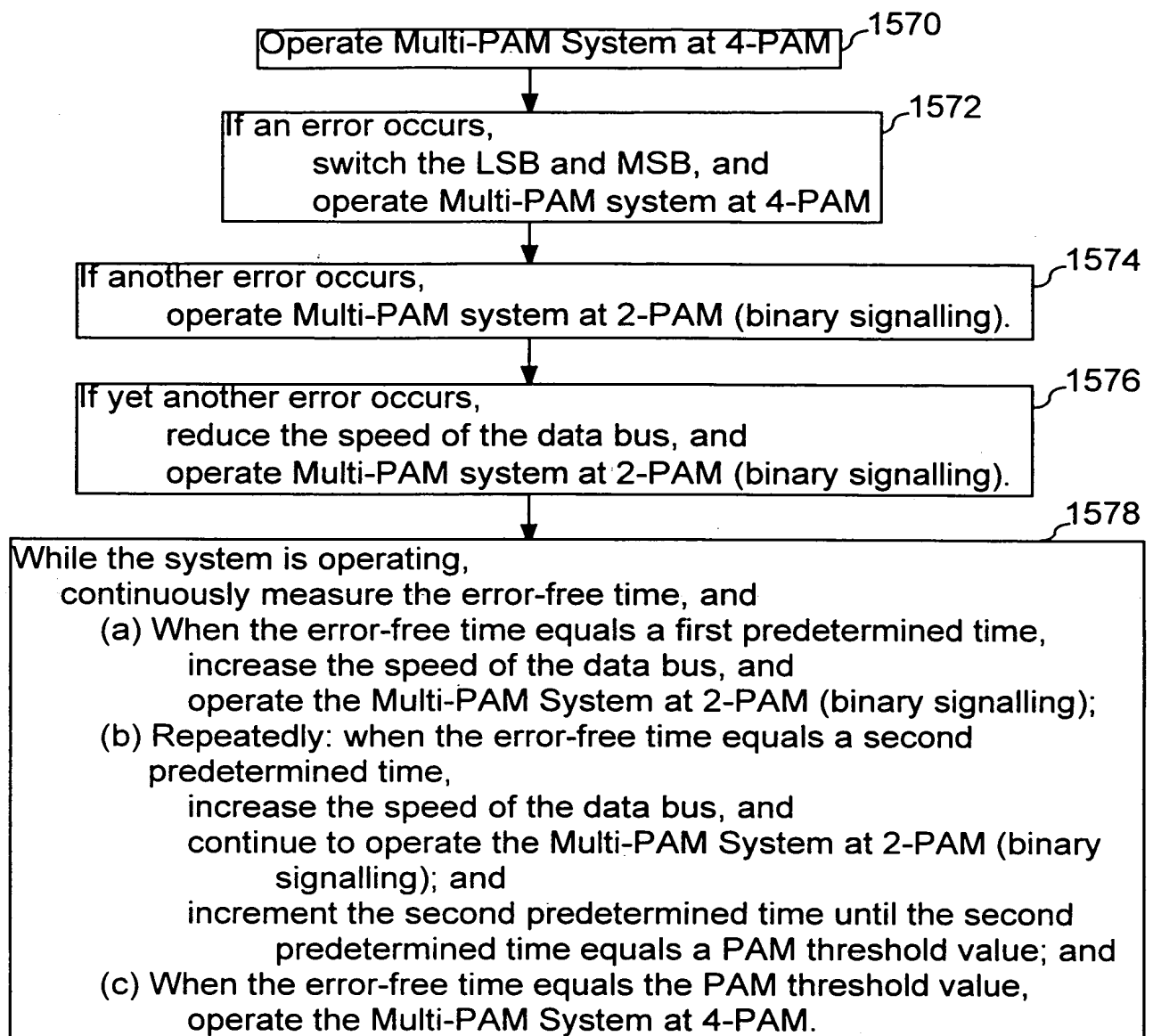


FIG. 57

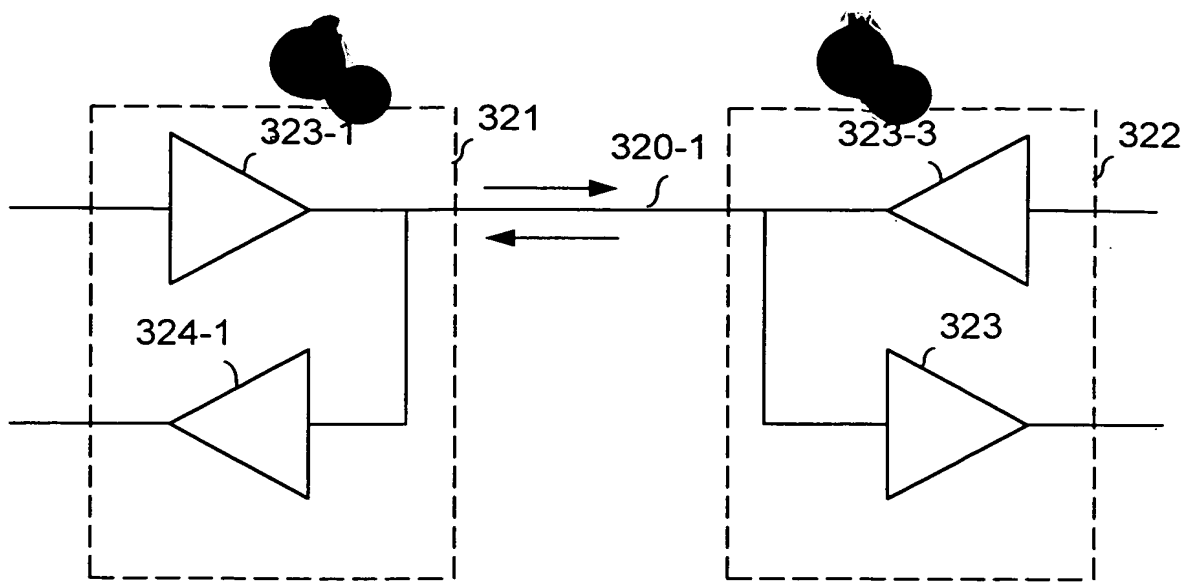


FIG. 58

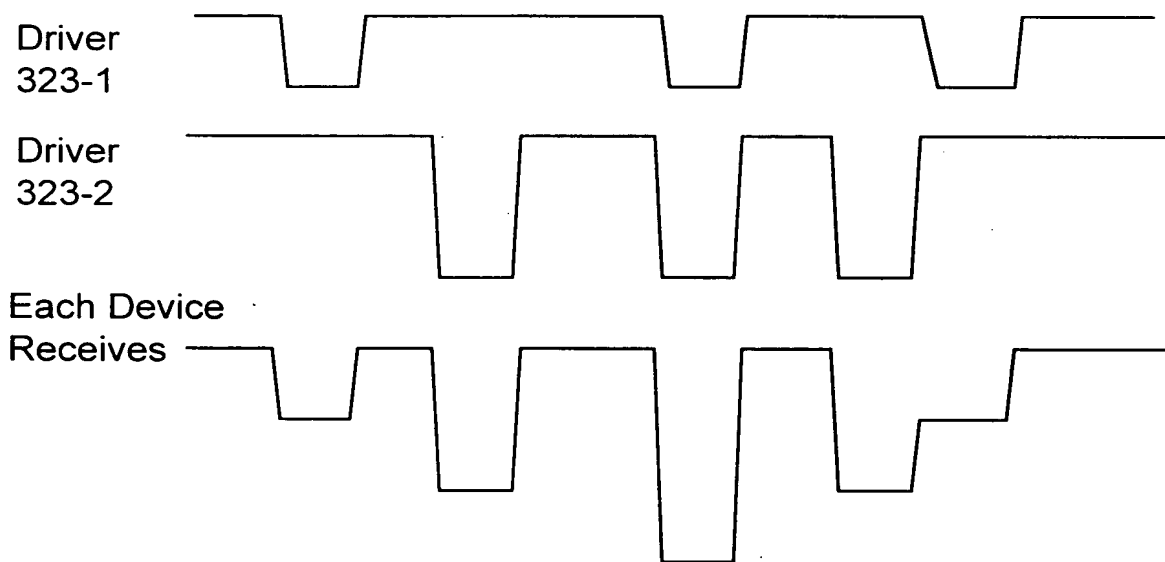


FIG. 59

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